Inhomogeneous Ring Oscillator for Within-Die Variability and RTN Characterization

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***Abstract*—This paper discusses the concept of an inhomogeneous structure for a ring oscillator (RO) to enhance the delay effect of a particular inverter stage. The frequency of the proposed inhomogeneous structure becomes a strong function of the inhomogeneous stage; thus, the variability becomes directly visible. With careful design of the inhomogeneous stage, the RO frequency can be made sensitive to a small set of transistors for characterizing transistor-by-transistor variability. Performance sensitivities of the transistors are enhanced more than 100 times that of other transistors in the RO. The proposed ROs are embedded into a 65-nm RO-array test structure, and it is verified that these ROs are highly sensitive to within-die local variability and random telegraph noise (RTN). The within-die local variability is then successfully decomposed into threshold voltage and gate length variations. Several characteristics of RTN have been successfully extracted with the proposed structure. The proposed structure is thus very useful for observation, characterization and modeling of static and dynamic transistor variations during switching operation.**

***Index Terms*—Process variation, RTN, ring oscillator.**

I. Introduction

WITH THE AGGRESSIVE scaling of process technology, not only static process variation but also dynamic variations such as RTN (random telegraph noise) [1] have become serious issues. During the introduction of a new technology, characterizing and modeling these variations is extremely costly [2]. Transistor performance and its variation need to be monitored regularly and fed into transistor models to correlate model-hardware.

Variation can be categorized into static and dynamic variation. Static variation is often called process variation because the variation occurs during the manufacturing process of a device. With technology scaling, process variation is increasing. Process variation can be further divided into D2D (Die-to-Die) and WID (Within-die) variation. WID variation can be random or systematic. Systematic components include layout dependent variability caused by metal-thickness variation in Cu-CMP [3], temperature variation during rapid thermal annealing [4], and stress variation in strained Si [5]. The random component is becoming larger with every new process technology node because of RDF (random dopant fluctuation) and LER (line edge roughness). Since 32-nm and beyond, new process technology, such as FinFETs and SOI MOSFETs are considered to be the alternatives for the planar bulk MOSFET. Undoped FinFETs and SOI MOSFETs do not have RDF-induced random variability. However, sources of variability, such as LER and metal gate granularity [6], contribute to variability. For any process, WID variability needs to be characterized accurately in order to reduce design margins. Often, these variations are expressed in terms of threshold voltage and gate length variations, as they are the dominant sources of variation.

Extracting accurate variation information for key process parameters of transistor threshold voltage and gate length is a huge challenge. One method is to use a device-array test structure and measure the variability of each transistor performance [7]. This is the most basic method, but implementation, measurement, and analysis is very costly. Ring oscillator (RO)-based structure can be used as process monitors for fast characterization. The advantage of RO is that the output frequency can be measured easily. In addition, implementation is easy and ROs can even be embedded onto product chips. ROs can be used to characterize process variability. An RO circuit reflects the switching behavior of MOSFETs, thus providing us with overall insight into the characteristics of digital circuits. However, a disadvantage to using ROs is that there is only one observable parameter, which is the function of many factors. Conventional RO frequency fails to give accurate information on a particular source. The inverter structure in an RO can be modified to sensitize the output frequency to a particular process parameter [8]–[10]. This paper advances the state-of-the-art by proposing an inhomogeneous RO structure where the RO frequency is sensitive to only a small set of transistors. The sensitivities are also enhanced more than 100 times that of conventional structures. Thus, accurate characterization of transistor-by-transistor variability becomes possible.

With aggressive scaling, dynamic temporal variation such as RTN is becoming a serious threat. RTN has already become a

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serious issue for SRAMs [11]. Measurement, analysis, and characterization of several statistical properties are needed to model the effect of RTN on circuit performance. Device level measurements are being conducted where DC bias is applied [12]. However, in order to characterize the RTN effect on circuit performance, the device's switching characteristic is more important. Therefore, the effect of RTN on devices under the switching condition need to be monitored and characterized as well for correlation to the DC measurement results. Recently, the effect of RTN during circuit operation has been reported [13]. Conventional RO circuit is used to measure RTN in this approach. In order to model the effect of RTN, the following properties are needed. *a*) Time constant of capture and emission time and *b*) Amount of threshold voltage shift.

Due to the lack of sensitivity for a conventional RO structure, it is difficult to measure the above properties accurately under the presence of noise. As RTN occurs at the device level, conventional RO fails to give us in-depth information on the transistor level fluctuation because the observable frequency contains characteristics of all transistors. Using our proposed inhomogeneous ROs, the above parameters can be observed and measured accurately, first because of the high sensitivity and second because of the sensitivity toward a small set of transistors.

The benefits of our proposed inhomogeneous RO can be summarized below.

1) Increased sensitivity to variation ⇒ increased visibility.
2) Sensitive to a particular transistor ⇒ Easy characterization and modeling.
3) In-situ measurement of RTN.
4) Digital ⇒ Easy to implement and measure.

This paper is an extension over [14]. The key extensions are summarized below.

1) Detailed explanation and operation of inhomogeneous RO.
2) WID random variability extraction method.
3) Extraction of several RTN parameters, such as emission and capture times.

The remainder of the paper is organized as follows. In Sec. II, the inhomogeneous RO structure is explained. Design examples of inverters suitable for creating an inhomogeneous RO are shown. A test chip is fabricated to validate our proposed ROs. In Sec. III, the structure of our test chip and our measurement procedure are explained. Measurement results of WID variability and RTN are also shown in this section. In Sec. IV, using the WID variability measured from the inhomogeneous ROs, several sources of variation are extracted. The extraction method and its validation are explained in this section. In Sec. V, the extraction of RTN parameters is demonstrated. Sec. VI concludes our paper.

II. Inhomogeneous RO Structure for Variability Enhancement

In this section, we first describe the concept of our inhomogeneous RO structure. Some design examples for the inhomogeneous inverter element are presented. A suitable structure for WID variability and RTN measurement is proposed. The discussions are all supported by SPICE simulations. A commercial 65-nm process is assumed in the simulation.

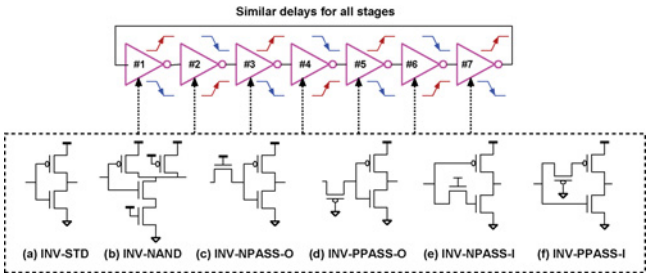

Fig. 1. Conventional seven-stage RO structure where the same type of inverter structures are used for all stages. As the RO oscillation period is the sum of each inverter stage delay, variation in a particular stage is not directly visible.

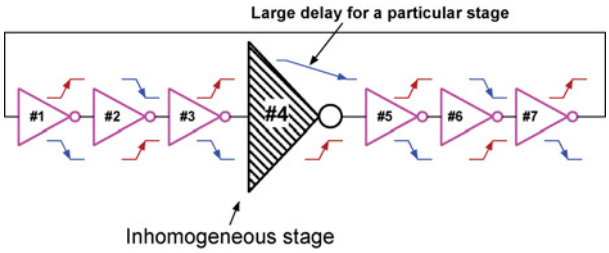

Fig. 2. Proposed inhomogeneous RO structure. A particular stage is designed to have a large enough delay compared to other stages so that the output frequency is a strong function of that particular stage's delay. Any variation in the inhomogeneous stage becomes directly visible to the output frequency.

A. Basic Concept

Fig. 1 shows a conventional RO structure where an identical inverter structure is used at all stages. Simple inverter cells or other logic gates such as NAND are used to capture variation and process characteristics. In such cases, the characteristics of all the transistors are averaged out and only one output observable parameter that is the RO frequency is measured. This frequency gives us a general idea of the underlying process characteristics. In order to capture WID random variability, multiple instances of the same RO type are measured. The distribution of the RO frequency gives us the amount of random variation, but fails to give us information of the underlying causes of variation. Several modified inverter structures are proposed in [15], [16] to extract detailed information on the underline variation causes such as threshold voltage and gate length. Even though we can get considerable information from the conventional homogeneous ROs, it is difficult to characterize dynamic variations like RTN, as these variations occur at the transistor level.

In this section, an inhomogeneous RO structure is proposed that enhances the sensitivity of RO frequency to a particular inverter stage delay multiple times more than its homogeneous counterpart. Furthermore, the number of sensitive transistors can be reduced to a small number, meaning transistor-by-transistor characteristics become possible. This enables easy

characterization and modeling of complex phenomena like RTN.

The basic concept is as follows. If the delay of a particular inverter stage or a transistor in a particular inverter stage is the dominant delay factor for the overall delay, the RO frequency becomes a strong function of that particular stage. Any variation in the inhomogeneous stage is directly visible to the output frequency. Thus, variability of the transistors in the inhomogeneous stage is enhanced. Fig. 2 shows an RO circuit with an inhomogeneous element. When a standard inverter, as shown in Fig. 1(a), is used for the inverter stages, it becomes a conventional homogeneous RO. If a pass-transistor loaded inverter, as in Fig. 1(c–f), is used for a particular stage and standard inverter for the remaining stages, it becomes an inhomogeneous RO. As will be shown later, the pass-gate loaded inverter stage becomes the dominant factor for the overall variation.

First, we explain our concept of inhomogeneous structure and its effect with the following simple approximations. Let the rise and fall delay of the ith stage in the conventional RO be T_{rise_i} and T_{fall_i}. The period of the RO oscillation T_{total} becomes as

$$T_{\text{total}} = \sum_{i}^{N} \left(T_{\text{rise}_i} + T_{\text{fall}_i} \right). \tag{1}$$

As shown in Fig. 2, the inverter cell of a certain stage is replaced by a special inverter cell whose fall delay is much larger than the other inverter cells. The period then can be rewritten as

$$T_{\text{total}} = \sum_{i}^{N-1} \left(T_{\text{rise}_i} + T_{\text{fall}_i} \right) + T_{\text{rise}_s} + T_{\text{fall}_s}. \tag{2}$$

$$1 = \frac{T_{\text{others}}}{T_{\text{total}}} + \frac{T_{\text{fall}_s}}{T_{\text{total}}}. \tag{3}$$

where, $T_{\text{others}} = \sum_{i}^{N-1} \left(T_{\text{rise}_i} + T_{\text{fall}_i} \right) + T_{\text{rise}_s}$. If the fall time of the inhomogeneous stage is the dominant delay component in the oscillation period, then Eq. (3) can be approximated as follows.

$$1 \approx \frac{T_{\text{fall}_s}}{T_{\text{total}}}. \tag{4}$$

Thus, the period becomes directly proportional to the fall delay of the inhomogeneous inverter. In the case of a homogeneous RO, the effect of delay variation in a particular inverter stage is reduced by the number of stages. In the case of an inhomogeneous structure, the effect of delay variation translates directly to the RO oscillation period; thus, larger sensitivity can be obtained as compared to the homogeneous structure.

B. Design of Inhomogeneous Element

In order to implement the idea of the inhomogeneous RO, inverter structures capable of creating inhomogeneity are required. In this section, one design example for the inhomogeneous element will be explained. We will further explore the design technique in our future work, and we expect others to come up with new circuit techniques.

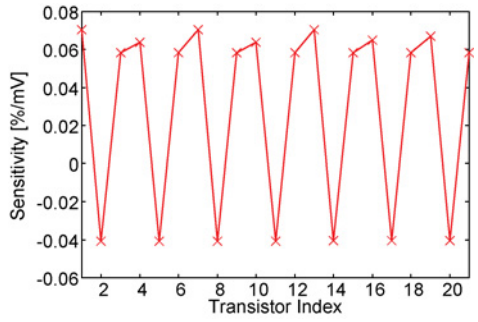

Fig. 3. Sensitivity of each transistor in a seven-stage homogeneous RO with conventional nMOSFET pass-gate loaded inverter. Similar sensitivities are observed for the MOSFETs in each inverter stage.

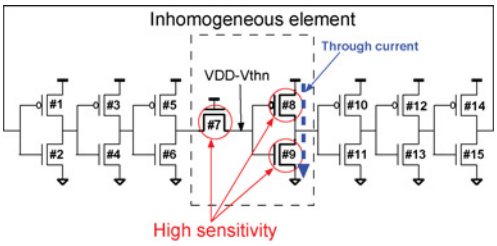

Fig. 4. Conventional pass-gate loaded inverter structure to create inhomogeneous element. RO frequency is sensitive to the three transistors in the inhomogeneous stage.

The design example that we used in our test chip is the one used by the authors in [10], [15] for enhancement of sensitivity to process variation. The conventional way is to make a homogeneous RO structure. For example, all the inverter cells in Fig. 1 are replaced by an inverter loaded with an nMOSFET pass-gate. We name this type of RO homogeneous "INV-NPASS-O" RO. Sensitivity of RO frequency to each transistor's threshold voltage variation is shown in Fig. 3. As expected, similar sensitivities are observed for the transistors in each inverter stage.

We now show the effect of inhomogeneity on sensitivity. Fig. 4 shows a seven-stage inhomogeneous "INV-NPASS-O" RO structure. Fig. 5 shows the sensitivity coefficient of each transistor in the RO for two different supply voltages of 1.2 V and 0.8 V. The pass-gate and the MOSFETs in the inhomogeneous stage have very high sensitivity compared to the others. At a nominal voltage of 1.2 V, the sensitivities of the pass-gate and the nMOSFET are 18 times larger and the sensitivity of the pMOSFET is seven times larger than the other transistors. This is because the voltage drop across the pass-gate increases the sensitivity of the pass-gate and the nMOSFET. The sensitivity of the pMOSFET increases because it remains partially on during the pull down, where it contributes largely to the delay . Reducing the supply voltage will increase the sensitivities of these MOSFETs drastically, as MOSFET performance becomes more sensitive with reduced gate over-drive. In Fig. 5, sensitivities of these transistors become more than 100 times as high as the others. With a pMOSFET-inserted inhomogeneous RO, the sensitivities are more than 40 times larger. Performance of inhomogeneous ROs is strongly affected by the variability of dominant transistors. This shows that the local variability of sensitive

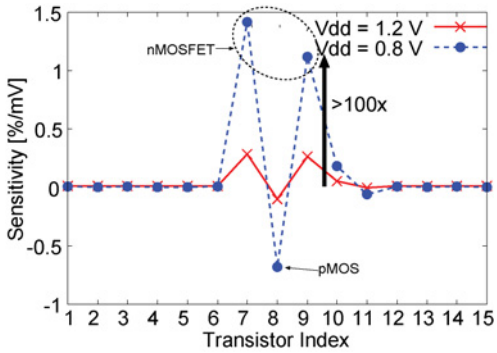

Fig. 5. Sensitivity of each transistor in a seven-stage inhomogeneous "INV-NPASS-O" RO of Fig. 4.

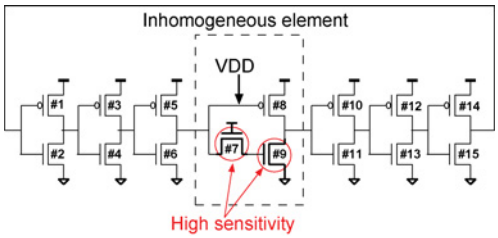

Fig. 6. Proposed pass-gate-based inverter structure for inhomogeneous element. RO frequency is sensitive to the nMOSFETs of the inhomogeneous stage only.

transistors can be estimated by measuring the inhomogeneous RO's frequency variability.

With a conventional pass-gate inverter structure as shown in Fig. 1(c) and Fig. 1(d), we can achieve more than 40 times greater sensitivity for three transistors in the inhomogeneous stages. These three transistors include both the pMOSFET and nMOSFET, which is not desirable when we want to observe variation on a particular type of device. We, therefore, have used a new inverter structure as the inhomogeneous stage to achieve higher sensitivities to either nMOSFET or pMOSFET only. Fig. 6 shows a seven-stage inhomogeneous RO with the new inverter cell as the inhomogeneous stage. We name this inverter the "INV-NPASS-I" and this RO as inhomogeneous "INV-NPASS-I" RO. Fig. 7 shows the sensitivities for each transistor in the RO for supply voltages of 1.2 V and 0.8 V. Only the pass-gate and the other nMOSFET in the inhomogeneous stage have higher sensitivity as compared to the "INV-NPASS-O" structure. More than 50 times sensitivity is achieved for the nMOSFETs only, thus characterization on the nMOSFET becomes possible. The pMOSFET-sensitive counterpart can be designed similarly. We name this RO the "INV-PPASS-I" RO. We omit discussion of "INV-PPASS-I" RO as the operation is just the opposite of the nMOSFET counterpart.

C. Number of Stages

Frequency sensitivity to a particular stage is reduced with the increase in number of stages. Fig. 8 shows the change in frequency sensitivities to individual transistors for an "INV-NPASS-I" inhomogeneous RO against the number of stages. The sensitivities are reduced by the number of stages. However, as the sensitivities for all transistors are reduced in the same proportion, the ratio between the sensitivity of inhomogeneous nMOSFETs and the sensitivity of other nMOSFETs remains constant at around 50. The number of stages has little impact on the observability of the transistor-by-transistor variability.

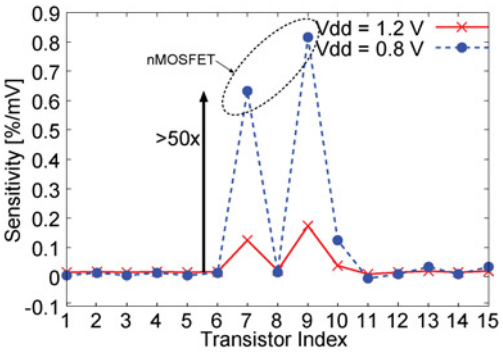

Fig. 7. Sensitivity of each transistor in a seven-stage inhomogeneous RO of Fig. 6.

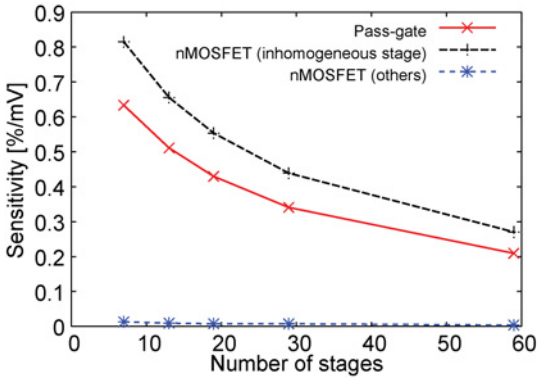

Fig. 8. Change of frequency sensitivity to individual transistor variation against the number of stages. Increase in the number of stages reduces the sensitivities of the transistors in the same proportion.

III. Test Chip Design and Measurement Results

A. Test Chip Design

A test chip in a 65-nm process technology has been fabricated. The process features one poly layer, 12 metal layers, copper wiring, and low-K insulating material techniques. The physical gate oxide thickness is 1.7 nm. In order to capture WID variability, the array-based test structure proposed in [17] is implemented. Fig. 9 shows the overall test structure. 294 RO clusters named "section" are arranged in an array of 14×21. The size of the RO-array macro is $1188\mu\text{m} \times 1267\mu\text{m}$. In order to avoid layout-dependent variability, layout of the section is hand-crafted. Each section consists of ROs of various types. Therefore, 294 ROs of the same type are integrated in a single die. We implemented homogeneous and inhomogeneous ROs. ROs consisting of standard inverter cell, nMOSFET-sensitive inverter cell and pMOSFET-sensitive inverter cell are designed. We implemented 13-stage and 19-stage ROs for both homogeneous and inhomogeneous ROs.

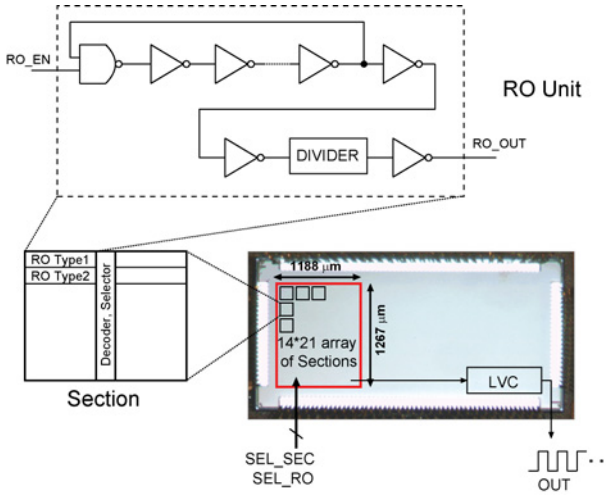

Fig. 9. Test structure to evaluate WID and RTN variability. Identical ROs are placed in an array of 14×21.

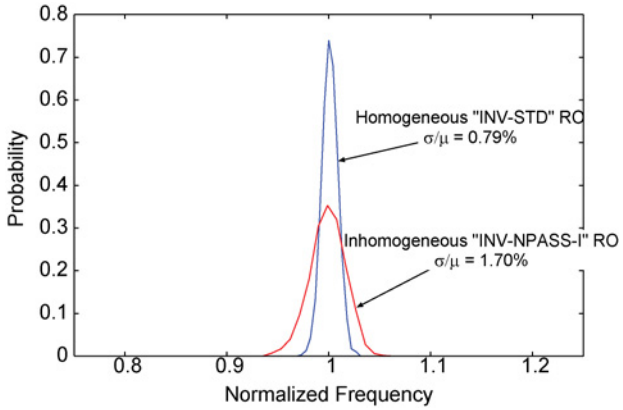

Fig. 10. RO frequency distribution at 1.2 V supply.

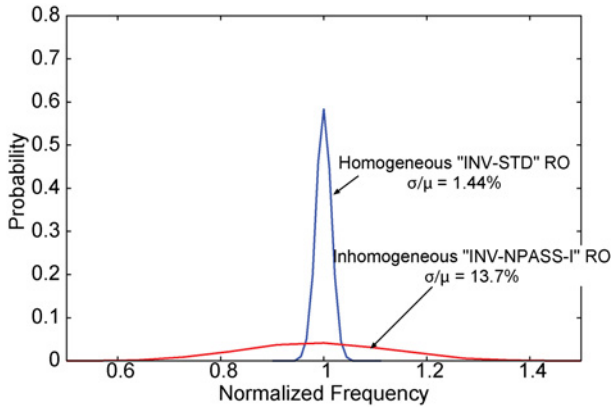

Fig. 11. RO frequency distribution at 0.8 V supply. Large variation is observed for inhomogeneous "INV-NPASS-I" RO.

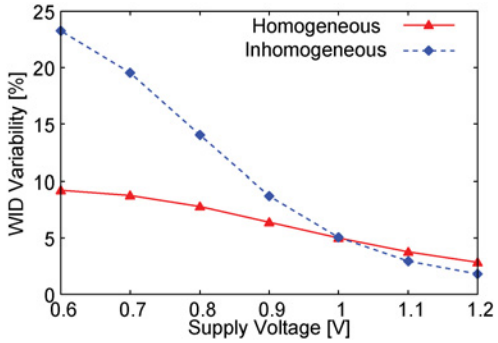

Fig. 12. Comparison between WID random variabilities of homogeneous "INV-NPASS-I" and inhomogeneous "INV-NPASS-I" RO at different supply voltages. The effect of inhomogeneity increases with decrease of supply voltage.

Selectors and decoders are used to select an RO to oscillate and capture the waveform outside the chip. A local divider and on-chip counter are used to reduce the frequency below one MHz so that the waveform does not get distorted outside the chip. Enable signals are generated locally inside the chip to avoid harmonic oscillation [18]. The number of stages for each RO is chosen at prime number 13 or 19 to minimize the probability of harmonic oscillation. We get 294 frequency measurements for a single RO; thus, WID variation can be obtained. Global variation can be obtained by averaging the 294 measured frequencies. We use homogeneous ROs to get global variations.

B. Measurement Procedure

The overall procedure for RO frequency measurement is as follows. First, an RO instance is enabled using the selectors. Then, the total time for a fixed number of oscillations is measured with a resolution of 12.5 ns using a 80 MHz clock signal. The number of oscillations is set to 1024 in our procedure. As the frequency outside the chip is around one MHz, the theoretical uncertainty of measured oscillation frequency in this procedure is $\pm 1/(1024 * 80) = \pm 0.001\%$, which is much smaller than the actual uncertainty due to jitter and noise. Then, the next RO instance is selected and measured. In order to check measurement precision, frequency of the same RO instance is measured 100 times. Variation for the 100 frequencies is 0.022%.

In order to characterize WID random variability, the systematic component is filtered out using the method in [17]. For RTN measurement, a single RO instance is kept oscillating for a certain period of time. Within that time, RO frequency is counted in every 20 ms.

In both WID and RTN measurement, supply voltage is varied. The nominal supply voltage is 1.2 V. From the discussion in Sec. II, supply voltage of 0.8 V is suitable for creating the inhomogeneity; thus, measurement results obtained at 0.8 V are used for analysis and characterization.

C. Measurement Results

1) *WID Variability:* We have 294 instances of the same RO type in the chip. From the 294 frequency measurements, we get a distribution. In order to show the effect of inhomogeneity on variability, measurement is done under two different supply voltages. Fig. 10 shows the frequency distribution for the inhomogeneous "INV-NPASS-I" RO along with the conventional homogeneous "INV-STD" RO frequency. Both the distributions are Gaussian, meaning that random variability is being observed. The standard deviations for the homogeneous and inhomogeneous ROs are 0.79% and 1.70% respectively.

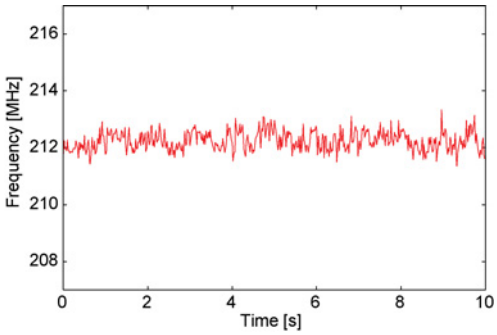

Fig. 13. RO frequency for an "INV-NPASS-I" inhomogeneous RO circuit over 10 s with small fluctuation (random noise) at 0.8 V supply.

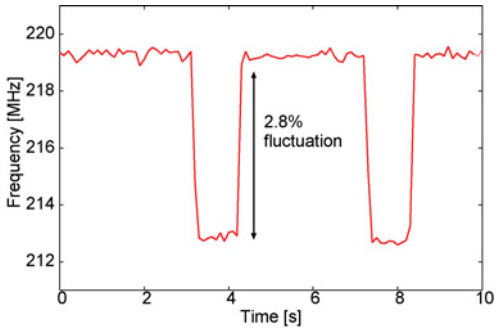

Fig. 14. RO frequency for an "INV-NPASS-I" inhomogeneous RO circuit over 10 s with binary fluctuation (RTN) at 0.8 V supply.

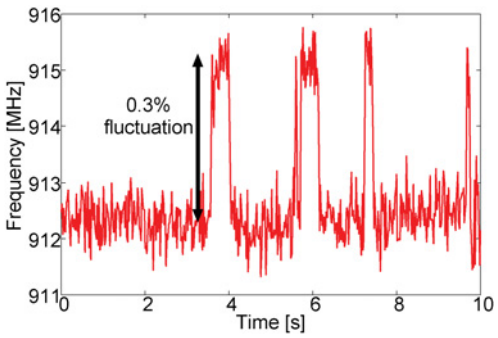

Fig. 15. RO frequency for an "INV-NPASS-I" inhomogeneous RO circuit over 10 s with binary fluctuation (RTN) at 1.2 V supply.

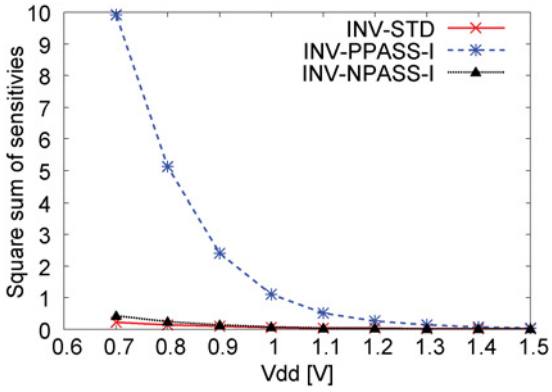

Fig. 16. Square sum of sensitivities to V_{thP} variation against supply voltage for different ROs.

Because the delay of the inhomogeneous stage is comparable to the other stages, little enhancement in variability is achieved at 1.2 V. In Fig. 11, the distributions for the two RO types are shown at a 0.8 V supply voltage. The standard deviations for these three ROs are 1.44% and 13.7% respectively. 9.5 times enhancement is achieved for the inhomogeneous RO against the homogeneous RO.

We next show the difference between homogeneous and inhomogeneous ROs with variation sensitive inverter cells (pass-gate cells) used in the homogeneous RO.Fig. 12 compares the WID random variability at different supply voltages. Below 1.0 V, the random variability of the inhomogeneous RO becomes dominant over the homogeneous RO. WID variability increases rapidly with decrease in supply voltage. This voltage dependency can be used effectively to extract the sources of variation. The extraction procedure and results will be discussed in Sec. V.

2) *RTN:* We measured the frequencies of 294 samples for every 20 ms at supply voltages of 0.8 V and 1.2 V. Fig. 13 and Fig. 14 show the measurement results of two samples for a 0.8 V supply. Most samples have small fluctuations on frequency, such as Fig. 13, which we consider random noise. However, we did observe a discrete fluctuation, such as Fig. 14, for five samples in the test chip. 2.8% frequency variability was shown at the 10 second measurement in Fig. 14. This discrete fluctuation has the characteristics of RTN and thus RTN has been observed. Fig. 15 shows the frequency fluctuation for the same RO circuit at a 1.2 V supply. 0.3% of binary fluctuation is observed. Larger fluctuation is observed at a reduced supply of 0.8 V because sensitivity becomes enhanced with reduced supply. Using the inhomogeneous RO, RTN dependence on supply voltage can be observed and characterized. We were not able to observe RTN-induced variability in any samples of homogeneous ROs. For homogeneous ROs, small fluctuations resulting from RTN in any of the transistors is not translated to the output frequency. Thus, it is very difficult to observe RTN-induced variability, let alone charactere and model it. As our proposed inhomogeneous RO translates small fluctuations of the sensitive transistors in the inhomogeneous stage, even the small fluctuation in threshold voltage is enhanced and becomes observable.

IV. Characterization of WID Variability

The proposed inhomogeneous ROs can be used for characterizing WID variability, as the frequency is sensitive to a small set of transistors. In this section, we show an example of using our inhomogeneous RO to extract WID random variability for threshold voltage and gate length from frequency variations. We use an estimation method based on a linear model of RO frequency to process variations. The method of building the linear models and details of the estimation procedure will be discussed. Finally, the estimation results will be presented.

A. Linear Model for Variability

In order to extract the sources of WID variability on real silicon, we develop a linear model. We assume that the sources of variability are limited to channel length L, and threshold voltage of pMOSFET (V_{thP}), and that of nMOSFET (V_{thN}).

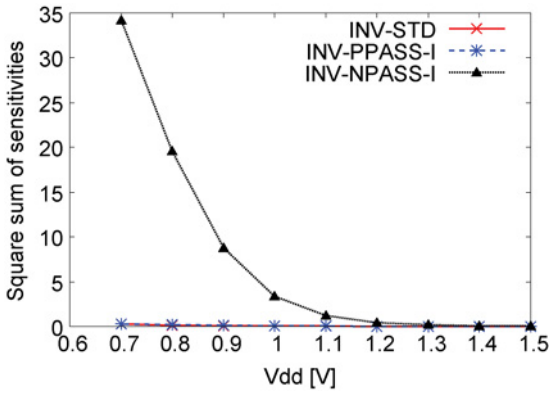

Fig. 17. Square sum of sensitivities to V_{thN} variation against supply voltage for different ROs.

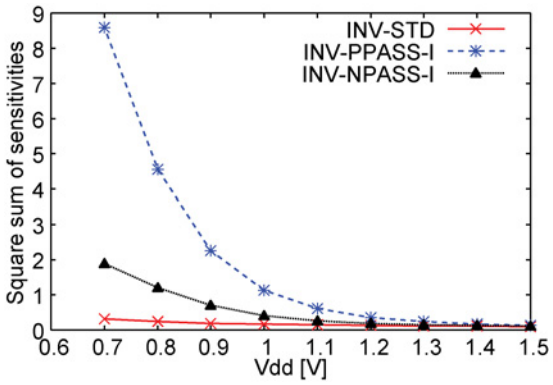

Fig. 18. Square sum of sensitivities to L variation against supply voltage for different ROs.

Assuming linear sensitivity of each variability source, the oscillation frequency variation, ΔF, can be expressed by the following equation considering only the first-order derivatives.

$$\Delta F = F - F_0 \approx \sum_i \left(\frac{\partial F}{\partial V_{\mathrm{thP}_i}} \Delta V_{\mathrm{thP}_i} + \frac{\partial F}{\partial V_{\mathrm{thN}_i}} \Delta V_{\mathrm{thN}_i} + \frac{\partial F}{\partial L_i} \Delta L_i \right). \quad (5)$$

Here, F_0 represents the nominal frequency when there is no variation, i is the transistor index in the RO, and $\Delta V_{\mathrm{thP(N)}_i}$ and ΔL_i are the amounts of variations in threshold voltage and gate length for the ith MOSFET. Sensitivity coefficients are calculated by circuit simulation.

We assume that the transistor variabilities are random and have no correlation to each other. The oscillation frequency variance is therefore expressed as the sum of variances caused by each random component, as follows.

$$\sigma^2_{\Delta F} = \sum_i \left(\left(\frac{\partial F}{\partial V_{\mathrm{thP}_i}} \right)^2 \sigma^2_{V_{\mathrm{thP}}} + \left(\frac{\partial F}{\partial V_{\mathrm{thN}_i}} \right)^2 \sigma^2_{V_{\mathrm{thN}}} + \left(\frac{\partial F}{\partial L_i} \right)^2 \sigma^2_L \right). \quad (6)$$

Here, $\sigma_{\Delta F}$ is the standard deviation of oscillation frequency, and $\sigma_{V_{\mathrm{thP}}}$, $\sigma_{V_{\mathrm{thN}}}$, and σ_L are standard deviations of V_{thP}, V_{thN}, and L variations, respectively. The validity of the above model will be discussed later in the section.

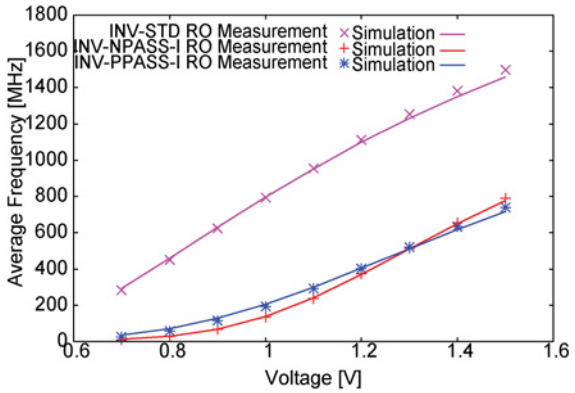

Fig. 19. Measured average frequency and simulated frequency of homogeneous ROs. Simulation is performed at the estimated center point in the process corner.

B. Extraction Method

By using the following two characteristics, we can extract the amount of variations for threshold voltage and gate length from the RO frequency variations. First we use different ROs having different sensitivities to the variation sources. Because of the high sensitivity toward nMOSFET and pMOSFET variation only, inhomogeneous "INV-NPASS-I" and inhomogeneous "INV-PPASS-I" ROs will be used. We also choose the homogeneous "INV-STD" RO, as this represents the characteristics of general logic circuits. Second we use the voltage dependency of the variation sources on the overall frequency variation. Fig. 16 to 18 shows the supply voltage dependency of variation sources for different RO structures. Fig. 16 shows the square sum of sensitivity coefficients to V_{thP} variation at different supply voltages. Sensitivity coefficients are calculated by circuit simulation. "INV-PPASS-I" RO shows large sensitivity compared to other ROs. Similarly, in Fig. 17, "INV-NPASS-I" RO shows large sensitivity compared to other ROs. In Fig. 18, "INV-PPASS-I" RO shows larger sensitivity to L variation than "INV-NPASS-I" RO. From Figs. 16 to 18, sensitivity to V_{thN} has a large supply voltage dependency, whereas sensitivities to other parameters have less. Using this difference of supply voltage dependency, we attempt to decompose frequency variation into the variations of process parameters.

The center point of linearization is an important consideration because the sensitivity values change depending on the center point. To determine the center point of linearization, we need to obtain center values for V_{thP}, V_{thN}, and L. Homogeneous ROs can be used to estimate the center values of V_{thP}, V_{thN}, and L for our target chip using the method described in [10].

In Eq. (6), unknown parameters that we want to derive are σ^2_{VthP}, σ^2_{VthN}, and σ^2_{L}. We can measure $\sigma^2_{\Delta f}$ at different supply voltages. Thus, we can build a system of linear equations using the three different RO structures described above. Using the system of linear equation, we can apply a least-square method to estimate the unknown parameters of our interest.

C. Estimation of Center Point

Homogeneous ROs of "INV-PPASS-I", "INV-NPASS-I" and "INV-STD" are measured for the target chip. The center values

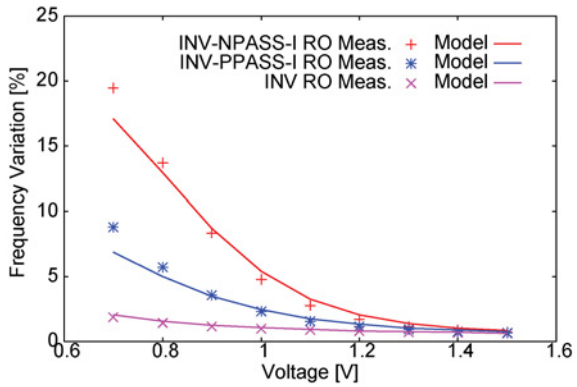

Fig. 20. Estimated frequency variations and measured frequency variations for three different ROs. Model Eq. (6) is used to estimate frequency variations using extracted variations of V_{thP}, V_{thN} and L.

of V_{thP}, V_{thN}, and L are estimated from the average frequency values for the three ROs.

Fig. 19 shows the simulated frequencies of three homogeneous ROs at the estimated center points of V_{thP}, V_{thN}, and L and measured frequencies. Simulated frequencies match with the measured frequencies at the supply voltage range of 0.7 to 1.5 V, confirming the validity of the estimation. The estimated center points are used to build linear models for extraction of WID variations.

D. Extraction of WID variability

We select a 19-stage homogeneous "INV-STD" RO, a 19-stage inhomogeneous "INV-NPASS-I" RO, and a 19-stage "INV-PPASS-I" RO for deriving variability of V_{thP}, V_{thN}, and L. WID random variations are measured for the target ROs over the supply voltage of 0.7 to 1.5 V. We then applied a least-square method for deriving the amount of variation in V_{thP}, V_{thN}, and L. The extracted standard deviations of V_{thP}, V_{thN} and L are 10 mV, 17 mV, and 0.9 nm, respectively.

E. Validation

The extracted amounts of variations in V_{thP}, V_{thN}, and L need to be verified. However, we do not have any reference on the actual variations in threshold voltage and gate length.

We, therefore, compare the frequency variation predicted by Eq. (6) using the extracted V_{th} and L variations with the measured frequency variation. Fig. 20 shows the predicted and measured frequency variations for homogeneous "INV-STD" RO, inhomogeneous "INV-NPASS-I" RO and inhomogeneous "INV-PPASS-I" RO. The solid line represents the predictions from the model. In Fig. 20, the predictions match closely with the measurements, even for extremely sensitive inhomogeneous ROs. Thus, we conclude that the amounts of variations in V_{thP}, V_{thN}, and L have been successfully extracted.

V. Characterization of RTN

RTN is considered to be a serious threat for future technology nodes. In order to ensure correct operation of circuits, RTN needs to modeled. In order to model RTN, the following parameters are needed.

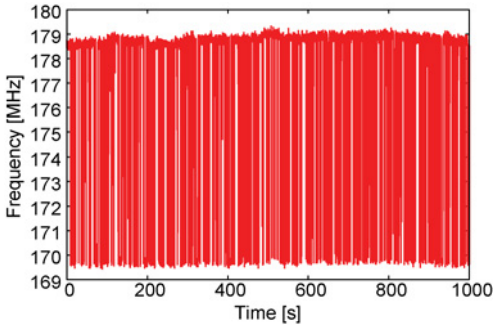

Fig. 21. Frequency fluctuation over 1000 s for an inhomogeneous "INV-NPASS-I" RO at the 0.8 V supply.

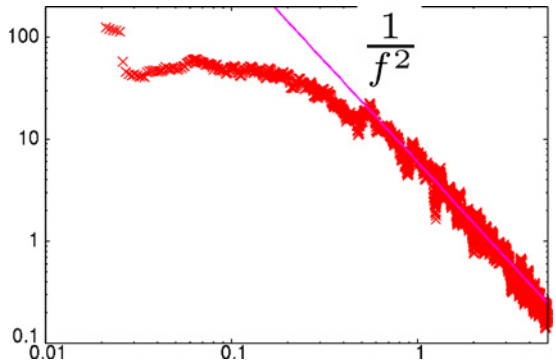

Fig. 22. Power spectrum density (PSD) RO frequency.

1) Time constant of capture and emission time, and
2) Threshold voltage shift.

Conventionally, devices are measured under DC bias to extract these parameters. The effect of RTN on digital circuits needs to be monitored and compared to the measurements obtained under DC bias. As shown in Sec. III, the proposed inhomogeneous RO shows large binary fluctuations because of the high sensitivity. Thus, the RTN effect becomes distinguishable. In order to extract the above-discussed RTN parameters, RO frequencies are measured for as long as 1000 s. Fig. 21 shows the frequency fluctuation of an inhomogeneous "INV-NPASS-I" RO at a 0.8 V supply voltage over 1000 s. Frequency is measured at every 50 ms in this case. Using the data, power density, time constants of capture and emission time, and threshold voltage shift will be extracted below.

A. Power Spectrum Density

Power spectrum density (PSD) is an important characteristic of RTN. We, therefore, have calculated the PSD of measured frequency fluctuation in Fig. 21. Fig. 22 shows the calculated PSD curve. The PSD fits with the $1/f^2$ curve, which is a sign that the observed fluctuation is RTN.

B. Time Constant

Emission time constant τ_e and capture time constant τ_c are two important parameters for RTN characterization and modeling. τ_e is the average dwell time of a carrier when it is trapped and waiting to be emitted, and τ_c is the average dwell time of a carrier when waiting to be trapped or captured.

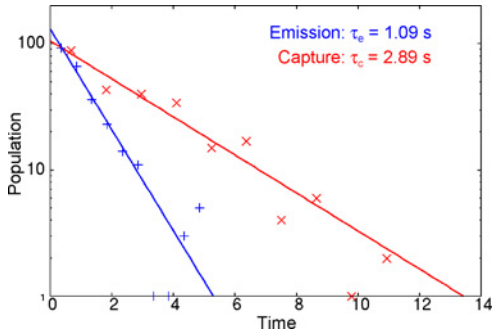

Fig. 23. Time constants of emission and capture time calculated from Fig. 21.

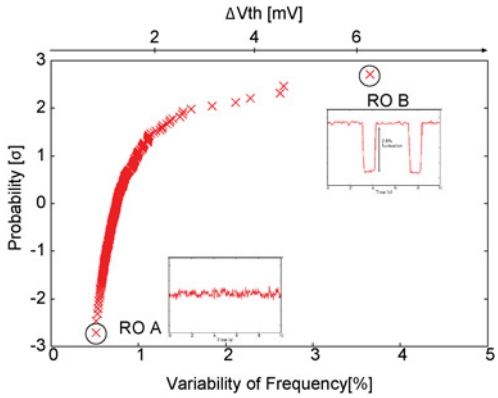

Fig. 24. CDF of RTN-induced threshold voltage variability.

These parameters depend on the trap position, trap energy, and bias condition. In order to measure these two parameters, statistical characteristics of the high V_{TH} state (carrier trapped) and low V_{TH} state (carrier detrapped) need to be measured. We therefore have measured the frequency of inhomogeneous "INV-NPASS-I" for a 1000 s period at a 0.8 V supply. From the measurement, time intervals between high and low V_{TH} states are calculated. Fig. 23 shows the distribution of time intervals measured. The X-axis is the time interval and Y-axis is the number of occurrences. The Y-axis is plotted in log scale. In Fig. 23, the distributions follow exponential fitting. This behavior agrees with the behavior for a single trap in a device [1]. From the exponential fittings in Fig. 23, the time constants of τ_e and τ_c are calculated to be 1.09 s and 2.89 s. Thus, the proposed inhomogeneous RO is extremely useful for characterization of RTN parameters because of the enhanced sensitivities.

C. Frequency and V_{TH} Shift Distribution

Fig. 24 shows a cumulative distribution function (CDF) of all the frequency fluctuations over 294 ROs. The vertical axis of the CDF is in log scale. As pointed out in device-level researches such as [12], RTN does not have a Gaussian distribution and a long tail exists for larger variability. Fig. 13 and Fig. 14 correspond to RO A and RO B in Fig. 24. The amount of frequency fluctuation can be converted into the fluctuation of threshold voltage using the sensitivity coefficient. The resulting V_{TH} shift is shown on the upper X-axis in Fig. 24. The maximum of the 6 mV V_{TH} shift is observed. This V_{TH} shift is an important parameter for modeling the effect of RTN. Exploiting the high sensitivity to a small set of transistors, the V_{TH} shift can be calculated. With the use of inhomogeneous ROs, we can characterize the effect of RTN on devices under switching conditions.

VI. Conclusion

In this paper, we discussed the concept of an inhomogeneous RO structure to enhance the sensitivities of a small number of transistors. By inserting an nMOSFET pass transistor into the RO structure, the sensitivities to the threshold voltage of two transistors become more than 100 times as high as that of others. We measured WID variability and RTN using an RO-array test structure fabricated in a 65-nm process, and revealed that the proposed ROs are sensitive to WID local variability and RTN. WID random variability is characterized and decomposed into three key parameters of threshold voltages and gate lengths. RTN-induced delay fluctuations are captured in the frequency of the proposed structure. The amount of fluctuation is then converted into threshold voltages exploiting the higher sensitivity achieved through the inhomogeneity. This structure is thus useful for accurate characterization of WID variability and RTN-induced variability.

Acknowledgments

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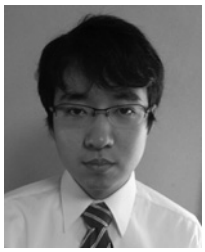

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