Reconfigurable Delay Cell for Area-efficient Implementation of On-chip MOSFET Monitor Schemes

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***Abstract*—To measure target MOSFET variation, specific monitor schemes are required. With device scaling, developing each monitor scheme is costly. This paper proposes a universal delay monitor cell which enables measurements of various types of variations with single monitor scheme. The monitor cell is reconfigurable and standard cell compatible; thus it can be used in the conventional place and route flow. An area-efficient monitor scheme to monitor global, local, and dynamic variations is developed. Measurement results from a 65-nm test chip shows the validity of the proposed monitor cell. The proposed cell enables area-efficient and low cost implementation of monitor schemes which can be integrated with application such as testing and adaptive voltage scaling.**

I. Introduction

Static process variations as well as dynamic variations such as random telegraph noise (RTN) is threatening the future scaling of MOSFET devices. New devices as FinFET and SOI MOSFET promises less manufacturing variability occurring from random dopant fluctuation. However, other sources of variation as line edge roughness, metal gate granularity, and interface trapped charges are contributing to variability [1]. Especially at low supply voltage, single charge based variability becomes visible. Accurate characterization and modeling of these variations are key challenges today.

Many process monitor schemes are proposed for characterization of variations [2–6]. Device-array based method is the most basic method [7], but this method is not suitable for fast characterization and on-chip monitoring. Several approaches are proposed to enable quick characterization [2–4], [8], [9]. In the existing monitoring techniques, measurement techniques differ depending on the target variation type. Many of them need sophisticated designs. In order to measure local random variability, large number of samples are required. For dynamic variations as RTN, device level DC measurement is performed. However, effect of RTN on logic circuits has gain much attention. Effect of RTN on ring oscillator (RO) frequency is reported [10]. In scaled devices, the effect of random variation, RTN, NBTI etc. on a particular device are becoming dominant. Thus, device level performance monitoring is required for accurate characterization. Furthermore, area-efficient implementation is required for embedding the monitor circuits anywhere in the product chip. Digital approach can reduce measurement cost and can further be integrated with adaptive techniques such as dynamic voltage scaling (DVS).

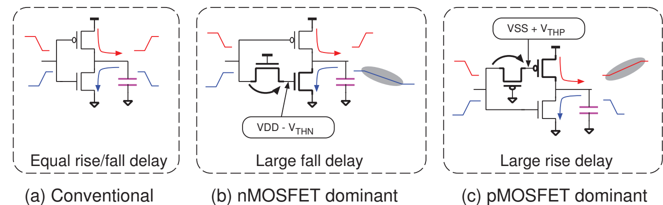

Fig. 1: Inverter cells used for MOSFET variation monitoring.

This paper proposes a universal delay monitor cell for on-chip measurement of MOSFET performance. The proposed cell is flexible and its delay can be configured. The proposed cell can thus be used as either standard cell, or pMOSFET-dominant cell, or nMOSFET-dominant inverter cell. Furthermore, the proposed cell has pair transistor structure enabling device level performance measurement. With the proposed monitor cell, monitor schemes can be built which can characterize various types of variations from a single instance. The proposed cell is digital, and can be used in the standard place and route flow saving design cost and complexity. In this paper, we demonstrate an all-digital monitor scheme where global variation as well as device level variations such as static random variation and RTN-induced dynamic variation are measured from a single monitor instance. The proposed monitor cell structure thus helps area-efficient and universal implementation of monitor schemes.

The remainder of the paper is organized as follows. In Sec. II, schematic of the proposed monitor cell and its operation are discussed. In Sec. III, the structure of a monitor scheme using the proposed monitor cell and the test chip design are described. Sec. IV demonstrates several measurement results to validate our proposal. Finally, we conclude in Sec. V.

II. Delay-configurable Universal Monitor Cell

A. Monitor Cell Structure

On-chip digital circuits to monitor transistor variation reduces measurement and design cost. RO is the most common choice because of its implementation and measurement advantage. Fig. 1 shows several inverter structures used in an RO. The first structure is conventionally used to monitor process characteristics. Due to the inability of differentiating pMOSFET and nMOSFET variations, inverter structures of Fig. 1(b) and Fig. 1(c) are proposed [8]. Using ROs consisting of these three types of inverter structures, measurement and estimation of several process parameters are possible [11].

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Inverter structures of Fig. 1(b) and Fig. 1(c) are reported to be useful for measurement of dynamic variations as RTN [9]. Inhomogeneous RO structure is used in their approach to enhance the variation effect of a particular stage. However, measuring several variation sources requires multiple designs of inverters as well as ROs. Furthermore, large instances of the same circuit are required for obtaining statistical properties. Instead of designing and implementing several monitor circuits of different monitor cell structures, we propose a universal monitor cell structure which can be used to monitor various types of variation by simply changing the delay behaviour.

Fig. 2 shows the schematic of our proposed monitor cell. The proposed cell is an inverter gate whose delay behaviour is configurable by signals. Different pull-up and pull-down paths can be configured in the proposed cell. Thus, the proposed structure gives flexibility on the implementation of monitor schemes. In Sec. III, we show how to implement a reconfigurable monitor structure using the proposed cell which is able to monitor even the local random variation and RTN-induced random variation from just a single instance. Table I shows several delay mode configurations for the proposed monitor structure.

pMOSFET dominant delay path is realized by turning OFF the C1 pMOSFET and the nMOSFET pass-gates, and turning ON the C0 nMOSFET and one of the pMOSFET pair pass-gates. nMOSFET dominant delay path is realized by vice versa. In order to implement the standard inverter, the following characteristics of the pass-gates are utilized. In Fig. 2, the output nodes of pass-gates become floating when both the pass-gates are turned OFF. When the input is at 'L', the output of the nMOSFET pass-gate pair becomes 'L' as well (Fig. 4) cutting the pull-down path completely OFF. Similarly, when the input is at 'H', the pMOSFET pass-gate pair output becomes 'H' cutting the pull-up path OFF. Thus, short-circuit current through partially ON pMOSFET and nMOSFET is avoided. During the switching operation, the output of pMOSFET pass-gate goes near to 'H' which in turn make the following pMOSFET OFF (Fig. 5). nMOSFET pass-gate similarly goes near to 'L' making the following nMOSFET OFF. During the switching operation, the standard inverter can be realized by turning all the pass-gates OFF.

The key idea is to use the pMOSFET pair and nMOSFET pair based pass-gate configuration. Each device in the pair can be either turned OFF or ON. The pair implementation gives us the following advantages. Firstly, by turning a single pass-gate ON and then swapping the pass-gate ON configuration, performance differences between these two devices can be measured. Secondly, while characterizing dynamic variations such as RTN, device level characterization is possible by re-configuring the pass-gates. Fig. 3 shows the rise and fall delays of the proposed cell for three different configurations at 0.8 V supply. The fall delay of nMOSFET dominant configuration and the rise delay of pMOSFET dominant configuration are multiple times larger than the standard inverter delays.

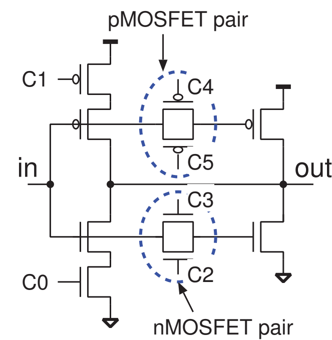

Fig. 2: Schematic of the proposed reconfigurable delay cell.

Table I: Delay configurations for the proposed monitor cell.

C5	C4	C3	C2	C1	C0	Delay Mode
1	1	0	0	0	1	Standard
1	1	0	1	0	0	nMOSFET-dominant (pass-gate 1)
1	1	1	0	0	0	nMOSFET-dominant (pass-gate 2)
1	0	0	0	1	1	pMOSFET-dominant (pass-gate 1)
0	1	0	0	1	1	pMOSFET-dominant (pass-gate 2)

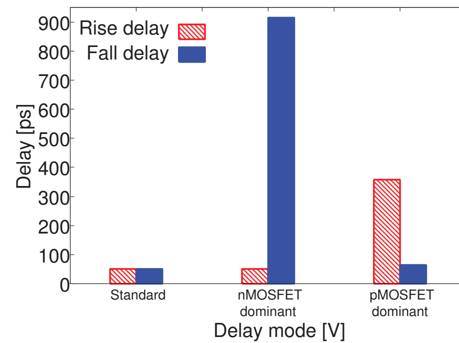

Fig. 3: Rise and fall delays of the proposed monitor structure for several delay modes at 0.8 V supply.

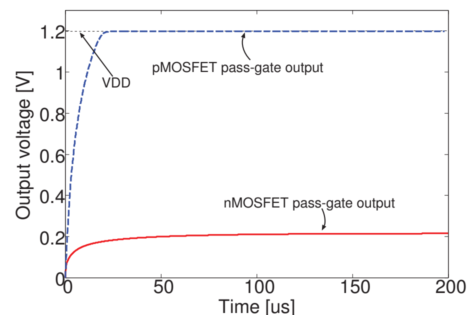

Fig. 4: DC characteristics of nMOSFET and pMOSFET pass-gate. Output voltages are set to 'L' initially. Then input is raised to 'H'.

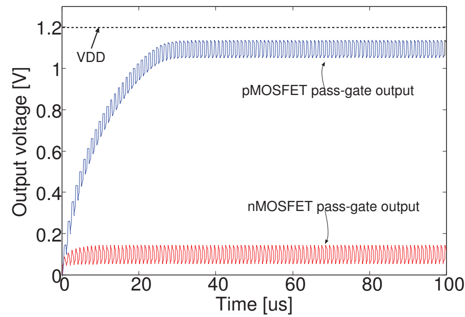

Fig. 5: AC characteristics of nMOSFET and pMOSFET pass-gates. Output voltages are set to 'L' initially. AC signal of 1 MHz is applied to the input.

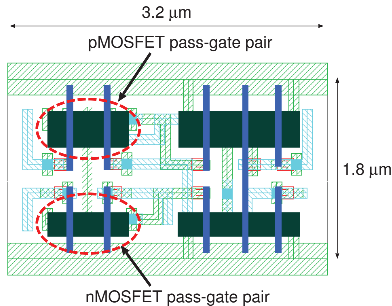

Fig. 6: Layout example of the proposed monitor cell structure.

B. Layout

Fig. 6 shows a layout example of our proposed monitor structure. The pair MOSFETs share the same source diffusion to minimize any layout induced variation. Thus, differences of pair MOSFET performances will give pure random variation. The size of the cell is 3.2 μm $\times$ 1.8 μm which is five times larger than the standard inverter cell. The monitor cell has the same height as the standard cells to facilitate conventional place and route design.

III. Monitor Scheme and Test Chip Design

A. Monitor Scheme to Measure MOSFET Variation

A monitor scheme is developed to measure several variations including statistical properties of random variation utilizing the flexibility and the universality of the proposed monitor cell structure. Fig. 7 shows the block diagram of the developed monitor scheme. The monitor scheme consists of a single RO of 127 stages. The proposed monitor cell is used as the inverting gate for each stage except the first one. An NAND gate used to control the oscillation. The scheme has a serial

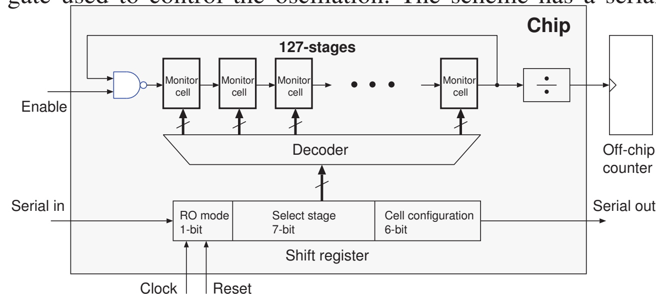

Fig. 7: Block diagram of the on-chip monitor test structure.

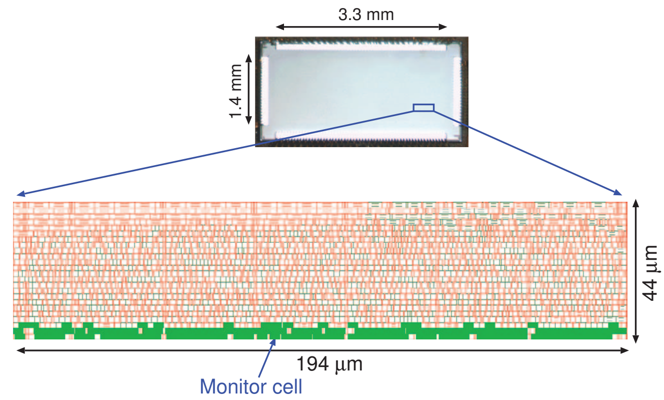

Fig. 8: Chip micrograph and layout of our developed area-efficient monitor scheme.

interface to set the values of a 14-bit shift register. A decoder decodes the shift register values and send configuration signals to each inverter stage. Independent configuration of each stage will give lot of flexibility but also increase design complexity. In order to reduce design complexity and area, the following selective configurations are implemented. For monitoring MOSFET performance inside a particular stage, the RO is configured to have inhomogeneous structure as proposed in [9]. One bit (RO mode) is used to configure the RO into a homogeneous structure or an inhomogeneous structure. For the homogeneous structure, the inverter cells can be configured to any of the delay modes as shown in Table I. Global variations in pMOSFET and nMOSFET can be measured with this configuration. For the inhomogeneous structure, only the inhomogeneous stage is set to be configurable with the cell configuration signal bits. Inverter stages other than the inhomogeneous stage are set to a default configuration which is the standard inverter cell configuration in this scheme. The inhomogeneous stage can be chosen with select stage signal bits. This way, 126 inhomogeneous configurations are achieved. By scanning all the inhomogeneous configurations and measuring their corresponding frequency values, statistical properties are derived.

B. Chip Layout

Fig. 8 shows the micrograph of our test chip and the layout of our developed monitor scheme. Standard cell based design is used. Automatic place and route is done which gives flexibility to embed the monitor scheme with any digital circuit. Highlighted cells show the proposed monitor cells. Area constraint is used for the monitor cell placement to avoid large capacitance at the output nodes. The area of the monitor scheme is (196 μm $\times$ 44 μm $=$) 0.0085 mm^2 which is only 0.18% of the whole chip area. With such a small area we can measure local static random variations, global variations and dynamic variations in each inverter stage.

IV. Measurement Results

A. Die-to-Die Variation

In order to obtain global variation, RO is configured into homogeneous structure. Frequencies are measured for each

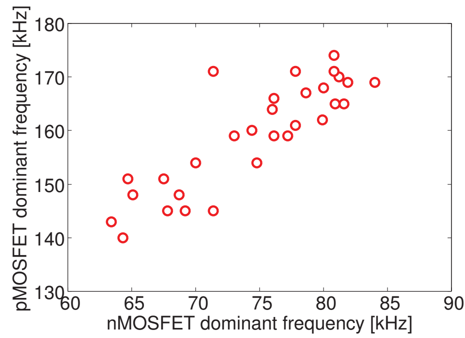

Fig. 9: pMOSFET-sensitive homogeneous RO frequency vs. nMOSFET-sensitive homogeneous RO frequency for 30 chips.

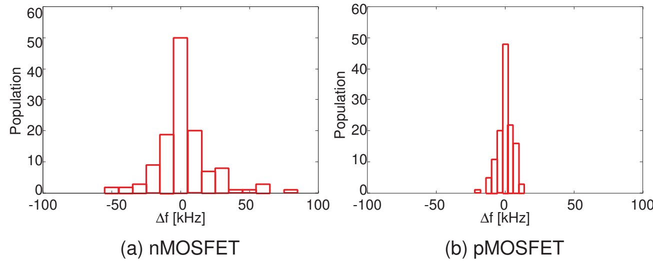

Fig. 10: Distribution of measured ΔF for nMOSFET and pMOSFET devices.

configuration of nMOSFET dominant path and pMOSFET dominant path. Fig. 9 shows the pMOSFET dominant frequency against the nMOSFET dominant frequency for 30 chips. Strong correlation is observed between D2D variations between nMOSFET and pMOSFET. Thus, the main cause for D2D variation is considered to be gate length variation.

B. Within-die Random Variation

Fig. 10 shows the distributions of measured ΔF for nMOSFET and pMOSFET pair pass-gates with inhomogeneous structures. Fig. 10(a) shows the distribution for nMOSFET and Fig. 10(b) shows the distribution for pMOSFET. nMOSFET random variability is larger than pMOSFET. Similar results are reported in device-level measurements [7]. Thus, the monitor scheme is able to detect random variation.

C. Random Telegraph Noise

Fig. 11 shows one sample of RTN-induced dynamic fluctuation of oscillation frequency. Discrete fluctuations are observed which indicates that RTN is being measured. 4 binary states are observed indicating two traps are involved. We could identify the devices with RTN.

V. Conclusion

In this paper, we proposed a universal delay monitor cell whose delay can be configured. The proposed monitor cell is digital and have very small area. Utilizing the pair transistor configurations, the monitor cell provides flexibility to implement area-efficient on-chip monitor schemes. An on-chip monitor scheme to monitor global variation, local random variation, and dynamic variations are developed. Measurement results from a 65-nm test chip validates the proposed monitor cell. The monitor cell is thus useful for on-chip monitoring

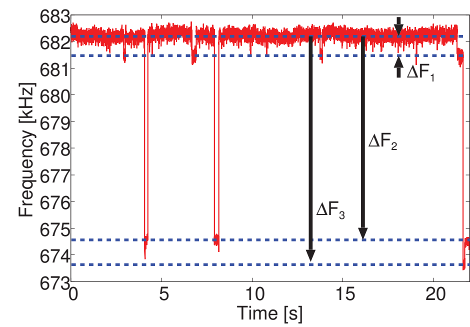

Fig. 11: Frequency fluctuation over time for an inhomogeneous configuration showing RTN-induced variation.

of statistical properties of transistor variations as well as transistor performances for various applications such as testing, adaptive voltage scaling etc.

Acknowledgments

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