On-chip Monitoring and Compensation Scheme with Fine-grain Body Biasing for Robust and Energy-Efficient Operations

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Abstract— Aggressive technology scaling and strong demand for lowering supply voltage impose a serious challenge in achieving robust and energy-efficient circuit operation. This paper first overviews on device-circuit interactions to enable cross-layer resiliency, and energy optimization. We show that the ability to monitor and control device and circuit characteristics not only increase energy-efficiency by more than 20% but also relax the severe design constraints, which were required because of the uncertainties of variability. We then demonstrate two proof-of-concept circuits in a 65 nm process to show variability resiliency and energy optimization with local body biasing.

I. Introduction

With technology scaling, variability is posing a great challenge on designing energy-efficient LSIs, as large amounts of margin need to be allocated in each layer of design hierarchy [1]. In order to utilize the full potential of a technology node, dynamic tuning of supply and threshold voltages based on PVT (Process, Voltage and Temperature) conditions as well circuit parameters have become a necessity now. Choosing the optimum supply and threshold voltages based on circuit's activity rate, operating frequency and logic depth can reduce the energy consumption compared to a fixed supply and threshold voltage operation [2]. However, the problem of today's design flow is that often the supply voltage and the threshold voltages are fixed. Circuit designers do not have any option to tune the threshold voltage for example. Furthermore, the use of large margins to deal with process variation results in the operation of the circuit with excess energy consumption. Transistor body biasing gives the designers an option to tune the threshold voltages [3], which can be used effectively to save large amount of energy. In order to apply body biasing technique for energy reduction, a design strategy along with an easy to implement hardware architecture is required. The problem gets complex when large device intrinsic characteristic variation as well as external parameter variations exist. This paper aims to ease this complexity and presents a simple but powerful approach with minimal hardware and design cost.

This paper focuses on the importance of having the ability from a circuit designer's perspective to monitor and control device characteristics particularly the threshold voltage. Firstly, we show that pre-defined target device characteristics can be achieved by self-adjustment of device threshold voltages with body biasing even when large process variation exists. Secondly, by tuning the threshold voltages of the devices their optimal values, large amount of energy saving is possible. On-chip monitors are required to monitor the deviation from the target values to self-adjust the process. Therefore, we need monitors with capability to track device characteristics instead of monitoring the critical path delay. However, critical path delay monitors can also be used for more robust operation. We first present a simple inverter based threshold and leakage monitors, and then demonstrate two proof-of-concept circuits to prove the concept of self-adjustment threshold voltages to their target values. First, a built-in self-adjustment circuit consisting of delay-line-based monitors and forward body bias generators to adjust the chip. Second, an AES cipher and decipher based self-testing circuit to demonstrate the energy reduction capability by optimizing the threshold voltage. Both the two circuits do not require any additional supply voltage and uses the clock signal only as its reference.

In Sec. II, we show that different circuit architectures require different sets of supply and threshold voltages for energy optimization. We then show the overall architecture of the self-adjustment system with multiple "substrate islands" where each "substrate island" having its own on-chip monitor based compensation scheme embedded. We also discuss on the simple inverter based monitors to track threshold voltage, leakage and temperature. In Secs. III and IV, we demonstrate two test chip results as a proof of our proposed concept. A built-in self-adjustment module is demonstrated in Sec. III, where the target device characteristics are achieved with on-chip feedback system. An AES-cipher-and-decipher-based self-testing module with built-in monitors and body bias generators are demonstrated in Sec. IV to show the importance of threshold voltage optimization. Sec. V puts our concluding remarks.

II. On-chip Monitors for Cross-layer Resiliency and Energy Optimization

A. Energy Consumption of LSI

Energy consumption of an LSI strongly depends on its circuit architecture such as logic depth, activity rate, operating frequency, temperature, etc. Here, we show that depending on

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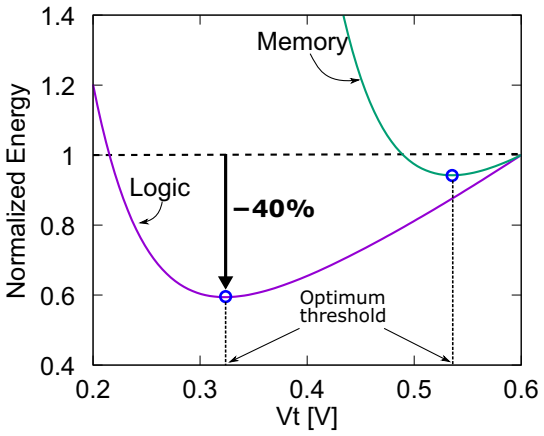

Fig. 1. Energy consumption of logic circuit and memory circuit against threshold voltage under a fixed delay constraint.

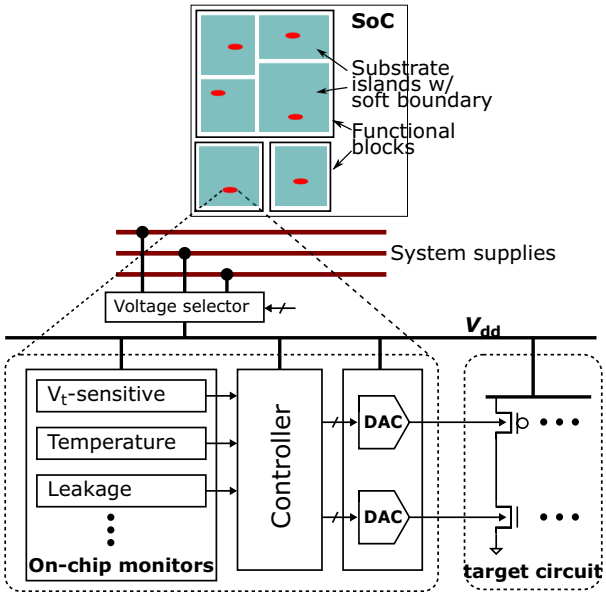

Fig. 2. A generic system architecture for energy optimization and variability resiliency with substrate islands.

the logic depth and activity rate, the optimum pair of supply voltage and threshold voltage ($V_{\rm dd}$, $V_{\rm t}$) differ largely under the same required operating speed.

The energy consumption of an LSI can be expressed as the following simplified form [4, 5].

$$E \propto {V_{\rm dd}}^2 \cdot \left(\xi + \frac{I_{\rm OFF}}{I_{\rm ON}}\right), \tag{1}$$

$$\xi = \frac{a}{L_{\rm DP}K}. \tag{2}$$

Here, η is DIBL coefficient, a is activity rate, $L_{\rm DP}$ is logic depth, and K is a fitting parameter. Here, the key parameter is ξ which represents the circuit architecture and activity rate . The OFF and ON currents of a transistor can be expressed by the following equations assuming subthreshold leakage as the dominant OFF current mechanism and sufficiently large gate over-drive for the ON state [6, 7].

$$I_{\rm OFF} = \mu C_{\rm ox}\frac{W}{L}(n-1){U_T}^2 {\rm e}^{\frac{-V_{\rm t}+\eta V_{\rm dd}}{nU_T}}, \tag{3}$$

$$I_{\rm ON} = \mu C_{\rm ox}\frac{W}{L}(V_{\rm dd}-V_{\rm t})^{\alpha}. \tag{4}$$

Here, μ is carrier mobility, $C_{\rm ox}$ is gate oxide capacitance per area, W is gate width, n is sub-threshold slope coefficient, and $U_{\rm T}$ is thermal voltage. α value of 1.3 is assumed. Using the above models, the energy consumption can be represented as following showing the relationship between supply and threshold voltages.

$$E \propto {V_{\rm dd}}^2 \cdot \left(\xi + \frac{(n-1){U_T}^2 {\rm e}^{\frac{-V_{\rm t}+\eta V_{\rm dd}}{nU_T}}}{(V_{\rm dd}-V_{\rm t})^{\alpha}}\right). \tag{5}$$

Energy consumption of two circuit architectures, which represent typical logic and memory circuits, are computed using Eq. (5) under the same delay constraint. Fig. 1 shows the normalized energy consumption of the two different circuit architectures. The reference point of 0.6 V is arbitrary here. The key point is that optimizing the $V_{\rm t}$ based on the circuit architecture can reduce large amount of energy compared with a fixed $V_{\rm t}$ value provided by the foundry. Note that the supply voltage is also scaled along with the $V_{\rm t}$ to keep the delay value constant here. ξ values of 10^{-2} and 10^{-4} are assumed to represent these two circuit types. For logic circuit, the optimum $V_{\rm t}$ is 0.32 V whereas that value is 0.54 V for the memory. This indicates that transistor threshold voltage needs to be scaled along with the supply voltage to optimize the energy consumption. A typical foundry often provides transistors with two $V_{\rm t}$ states only, although the designer may need a larger variety of $V_{\rm t}$ values. Hence, the controllability of $V_{\rm t}$ by means of body biasing can be an attractive option for the circuit designers. Recently, fully-depleted SOI processes offer a wider range of body biasing capability [8, 9] resulting in research activities on using body biasing effectively.

B. Proposed System Architecture

Fig. 2 depicts the concept of an SoC chip with on-chip monitor based local body biasing to minimize energy consumption. As both the $V_{\rm dd}$ and $V_{\rm t}$ need to be scaled for energy optmization for target block, $V_{\rm dd}$ needs to be tuned as well. Assuming output current required to charge the body potential does not fluctuate drastically, precise regulation of the body voltage is not required. Hence, on-chip embedded body bias generators will suffice the $V_{\rm t}$ tuning purpose. However, on-chip $V_{\rm dd}$ generators require precise regulation and their design is costly. thus mulptile supply voltage levels are required if not continuous as continous $V_{\rm dd}$ tuning might be too expensive. Furthermore, different blocks required different $V_{\rm dd}$ values. Instead, a discrete set supply voltages can be used in the system where multiple blocks will share a common supply voltage. On-chip monitors are used to track the threshold voltage changes so that the target value is achieved. Large circuit blocks are divided into several "substrate islands" and optimum threshold voltages are applied to each island separately to compensate the systematic variation as well.

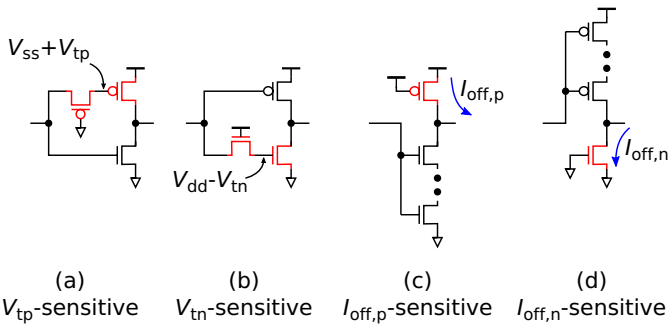

Fig. 3. V_t- and leakage-sensitive inverter delay cells.

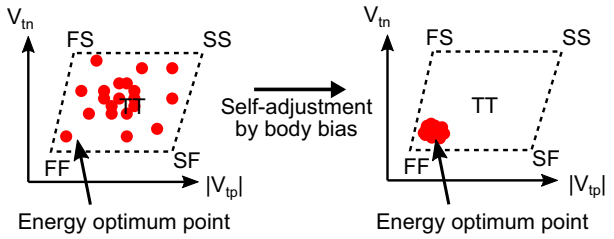

Fig. 4. Concept of self-adjustment of device threshold voltages to their energy-optimum values.

C. On-chip Monitors for Device and Circuit Characteristics

The key requirement to realize the system in Fig. 2 is to have small on-chip monitors that can propagate the device characteristic information to the circuit. Therefore, we focus on monitors that are capable of detecting device characteristics. Design-dependent critical path monitors [10–12] or in-situ timing monitors [13–15] can also be used in complementary with the device parameter monitors to increase the system robustness.

In order to embed the monitors into the target circuit seamlessly, we propose the following characteristics for the monitors.

1. Small area,
2. no analog interface,
3. digital calibration, and
4. capability of cell-based design automation.

A simple delay based monitor would meet all the above requirements. We have proposed several inverter cell topologies to facilitate delay based monitoring of various device characteristics [16–19]. We give a simple summary of our proposed monitor cells next.

C.1 V_t-sensitive Monitors

Four different topologies of an inverter cell are shown in Fig. 3 [16, 19]. The idea is to realize inverter delay which is highly sensitive to threshold voltage than those of the conventional inverter and other cells used in a standard cell library. One key point is to make the delay sensitive to either of the nMOS or pMOS transistors. Fig. 3(a) and Fig. 3(b) use pass-gate topology so that the gate–source overdrive is reduced by the amount proportional to the V_t value. Fig. 3(a) is sensitive to V_{tn} variation, and Fig. 3(b) is sensitive to V_{tp} variation.

C.2 Leakage and Temperature Monitors

Fig. 3(c) and Fig. 3(d) are proposed to monitor leakage current variation of nMOS and pMOS transistors independently [19]. In these topologies, either the pull-up or the pull-down transistor is turned OFF and the input is connected to either of the pull-down or pull-up path. As leakage current varies exponentially according to V_t or temperature variation, leakage monitor can also be used as a process and temperature monitor.

C.3 Monitor Architecture

Process-sensitive or temperature-sensitive inverter cells as shown in Fig. 3 can be used to form a delay line and then their delays will be calculated comparing to the clock signal. Another way of using the inverters to form a ring oscillator and measure its frequency with frequency counters. Again, clock signal can be used as a reference here. Delay-line based approach is more suitable for area-efficient implementation as frequency counters are not required. However, the controller in Fig. 2 can share a single frequency counter, and measure the monitor frequencies in a sequential manner. Either way, the monitor delays need to be pre-calibrated well so that the target delay is representative of the target device characteristics. The delay line topologies can be homogeneous or inhomogeneous [18] depending on our target monitoring parameter. The delay line can also be made reconfigurable for area-efficient implementation [20, 21].

III. On-chip Compensation Scheme For Process Self-adjustment

A. On-chip Compensation based Process Self-adjustment

In order to tune the threshold voltage of transistors by body biasing, the threshold voltage of the transistors need to be monitored. Otherwise, unnecessary tuning of V_t may occur causing large leakage consumption. Fig. 4 shows a conceptual illustration of the distribution of chip in the process space after fabrication without any V_t tuning. Now, let us assume that the optimum V_t values locate near the "FF" corner. We have chips near the optimum point, and chips far away from the optimum point. So, the amount of V_t tuning required for each chip to achieve the target optimum point differes largely between chips. One way to determine the adequate amount of body biasing is to use the IDDQ signature obtained during the testing [22]. This kind of technique however is not suitable for large SoCs where multiple functional blocks can share a common supply. Besides, this approach is only applicable for external voltage generators where we can tune the voltage regulation. Another drawback is that the difference between nMOSFET and pMOSFET threshold voltages can be distinguished. So, to realize the system in Fig. 2, we need embedded body bias generators. Hence, a self-adjustment scheme with the help of on-chip compact monitors will provide adequate V_t tuning for each "substrate island". Taking the conceptual example of Fig. 4, the self-adjustment scheme will adjust each chip automatically to the target optimum point. A speed-adaptive body bias generation [23] where

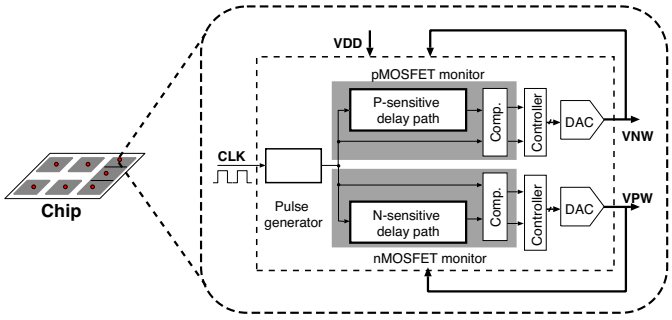

Fig. 5. On-chip fine-grain process variation compensation using separate pMOS- and nMOS-sensitive delay paths.

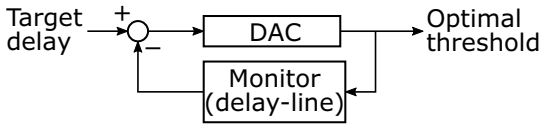

Fig. 6. On-chip feedback system using DAC and monitor to ensure target threshold is achieved.

the body bias voltages are generated adaptively based on the circuit speed. A threshold voltage balancing scheme [24] is also proposed to balance the threshold voltage differences between nMOSFET and pMOSFET using a logical threshold detector. Here, we focus on the digital delay-line-based approach and show how the device threshold voltages can be tuned automatically to achieve the target values.

B. Built-in Compensation Scheme

We show an example of a built-in self-adjustment scheme to adjust the transistor V_t to a pre-defined target value. Fig. 5 shows the overall scheme of out self-adjustment architecture. The proposed scheme divides the target circuit block into small regions called "substrate islands". The size of a "substrate island" is flexible and can be small as 0.1 mm^2. The monitoring part of the circuit detects performance of nMOSFET and pMOSFET independently. The target V_t is set during the design phase by setting the delay value accordingly. Body voltage of each "substrate island" is adjusted to compensate any deviation from the target delay set for each monitor. Fig. 6 shows such a feedback system to achieve the target V_t values for nMOS and pMOS transistors. As on-chip monitors are used to constantly track V_t changes, feedback based system has the potential to compensate transistor aging as well.

The right part of Fig. 5 illustrates the circuit configuration of the self-monitoring and compensation circuit. Two DACs (Digital-to-Analog Converters) supply n-well and p-well bias voltages so that the performance of each type of transistors meets the target. The self-monitoring and compensation circuit works only with a core supply and a system clock, and it can be implemented in a cell-based design so that it can be embedded in a target circuit under compensation.

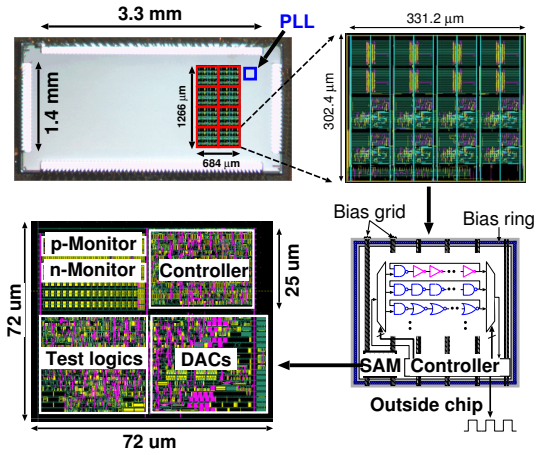

Fig. 7. Layout of the implemented on-chip monitoring and compensation scheme in a 65 nm process.

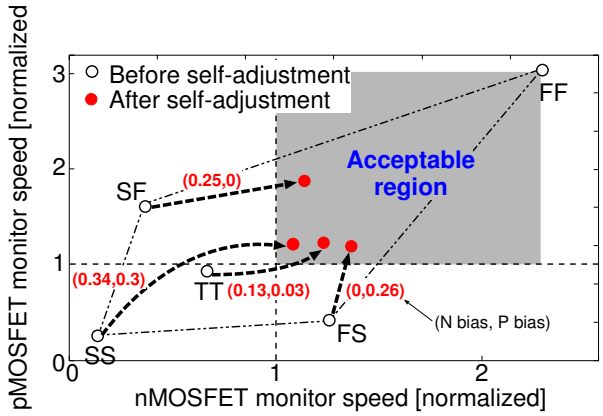

Fig. 8. Output performances of pMOSFET-sensitive and nMOSFET-sensitive ROs. Performances are measured before and after self-adjustment. Generated body biases for each corner are shown in the closed brackets.

C. Implementation Example in a 65 nm Process

We have implemented an example built-in self-adjustment circuit in a 65 nm process [17]. Fig. 7 shows the layout of the chip where 8 "substrate islands" are placed. Each "island" contains delay-line based P/N-monitors, DACs to generate n-well and p-well voltages, controller, and various ring oscillators to measure the delay of different logic gates. A cell-based automatic design procedure is adopted for the DACs too [25], thus the whole circuit can be embedded anywhere within the target digital circuit block. The target supply voltage is set to 0.7 V, and the delay values are set such that the delay meets the "TT" process corner. In this example, only forward body biasing is implemented. However, reverse body biasing can be easily adopted by making DACs compatible to reverse biasing as well [26].

D. Measurement Results

Chips targeting 5 process corners of "TT" (nMOSFET,pMOSFET), "SF", "FS", "SS", and "FF" are fabricated to demonstrate to self-adjustment capability. Fig. 8 shows the

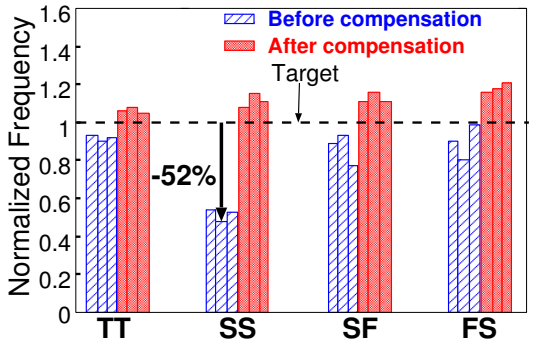

Fig. 9. Gate delay of NAND2 cell.

measured delays of the P/N-monitors before and after the self-adjustment. Before the self-adjustment, the monitor delays are located near the five separate process corners. After the self-adjustment is turned ON, the monitor delays are adjusted automatically by self-generated body biasing so that the delays targeting the a specific point in the process space is met. As only forward bias generation is implemented in this demonstration, chips locating on the top-right part of the process space are left as it is. Implementing bias generators capable of genering reverse biasing also can compensate those chips as well, and we can obtain the self-adjustment as shown in Fig. 4. The target point can be set by adjusting the delay values accordingly.

Next, delay values of several logic gates are measured to confirm the adjustment of actual path delays. Fig. 9 shows the measured delay values for NAND logic gates. Before the self-adjustment, NAND delays at "SF", "FS" and "SS" corners do not meet the target delays, whereas after the self-adjustment all the delays meet the specification.

IV. Energy Optimization by Fine-grain Body Biasing

As shown in Fig. 1, optimum set of $V_{\rm dd}$ and $V_{\rm t}$ differs under a fixed delay constraint based on circuit architecture, activity rate, and the delay value itself which is the operating frequency of the circuit. In this section, we prove the theoretical assumption of Fig. 1 for logic circuits only with silicon measurement results using an AES cipher/decipher logic circuit implemented in a 65 nm process. For cost- and area-efficient implementation, a built-in body biasing approach is taken such that no external interface is required. In this demonstration though, we have added digital interface to tune the body biasing value externally but this is not a must requirement. As explained in the previous section, the target $V_{\rm t}$ value can be set by setting the delay values of the monitors accordingly.

A. Built-in Body Biasing for Cost- and Area-efficient Implementation

A.1 Demonstration Circuit in a 65 nm Process

A test chip is fabricated with a 128-bit AES cipher/decipher core in a 65-nm low power triple-well bulk process. The block diagram of the AES cipher/decipher core is shown in Fig. 10.

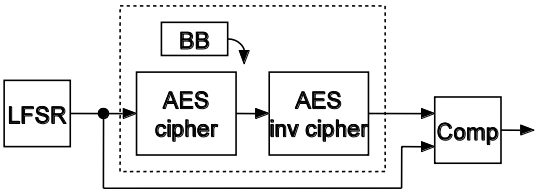

Fig. 10. Block diagram of self-testing module consisting of AES cipher and decipher modules.

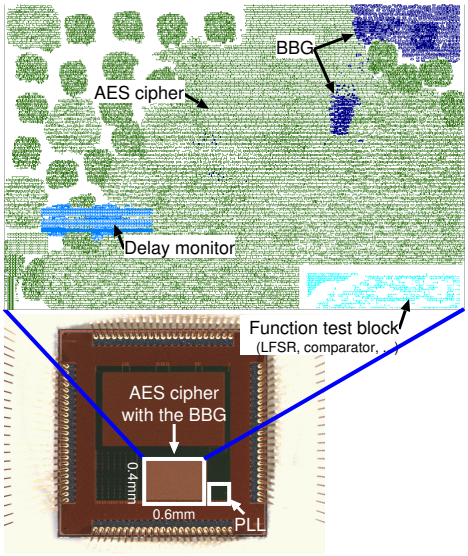

Fig. 11. Layout of an AES cipher and decipher module with built-in monitors and body bias generators.

The micro-graph and layout of the chip are shown in Fig. 11. A boby bias generaotr (BBG) module is integrated with the AES cipher/decipher core. The area of the AES cipher/decipher core including the BBG and the comparison circuits is 0.22 mm^2. The area required for the BBG is only 0.0052 mm^2, thus the area overhead of the BBG is 2.3%. The BBG is capable of generating both of the RBB and FBB. The AES core also includes several delay monitors consisting of inverter cell presented in Fig. 3 to evaluate circuit performance and device characteristics. Physical layout of the BBG and AES core is designed by EDA tools as shown in Fig. 11. The BBG design can be made parameterized for its flexible implemetation based on the target "substrate island" area. The AES core was synthesized using the foundry provided standard cell. The nominal supply voltage is 1.2 V and the maximum clock frequency achieved during the design is 400 MHz. Table I summarizes the specification and design constraints of the implemented AED cipher/dechiper module.

A.2 Measurement Results

Fig. 12 shows the Shmoo plot of the AES core. (a) region in Fig. 12 shows the passed combination of operation frequency and supply voltage. (a) + (b) region shows the area where correct operation has been achieved when body biasing is also applied. Increase of operating frequency and lowering of supply

TABLE I
SPECIFICATION AND DESIGN CONSTRAINTS OF THE AES CIPHER/DECIPHER MODULE.

Process	65 nm bulk CMOS
Supply voltage	1.2 V
Frequency	400 MHz
Gate count	28 k
Area	0.6 mm × 0.4 mm

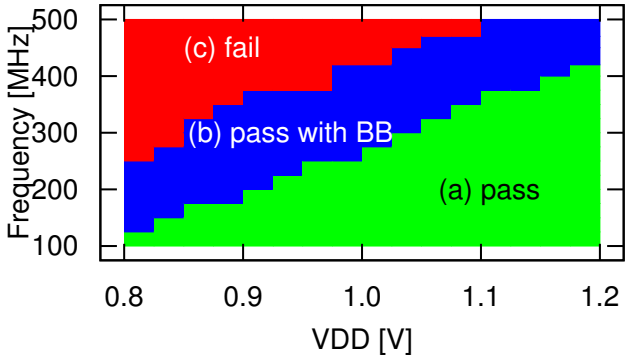

Fig. 12. Shmoo plot of the AES cipther/decipher self-testing module. Maximum of 0.6 V of forward body bias is applied.

voltage have been confirmed by applying body biasing. For example, the target operating frequency of 400 MHz is achieved by lowering the supply voltage down to 1.14 V when no bias is applied. However, when supply voltage and body bias is tuned simultaneously to find the minimum energy operation, the supply voltage is reduced to 0.96 V. As we are using a bulk CMOS process and maximum forward bias value of 0.6 V could be applied. It is found that the energy optimum $V_{\rm t}$ is achieved at this maximum forward body bias value. Using an FD-SOI process, the amount of forward biasing can be increased further to find the minimum energy point.

Fig. 13 shows the average energy per cycle measured for different frequency operation. At 400 MHz, the reduction rate of energy consumption with both the $V_{\rm dd}$ and $V_{\rm t}$ scaling is 20% compared with the $V_{\rm dd}$ scaling alone. As only a single supply is used, the energy consumption shown here includes the energy consumption of the BBG as well. At 200 MHz of frequency operation, 24% of energy reduction has been confirmed. The measurement results show that scaling $V_{\rm dd}$ and $V_{\rm t}$ simultaneously achieves more energy-efficient design. Body biasing can be used as an effective means to control $V_{\rm t}$ value to a pre-defined target value with the help of on-chip monitors.

V. CONCLUSION

In this paper, we have discussed on the use of on-chip monitors combined with body bias based compensation to minimize energy consumption and design margins. We have shown that for delay constrained logic circuits, reducing the threshold voltage to enable supply voltage reduction is necessary for energy

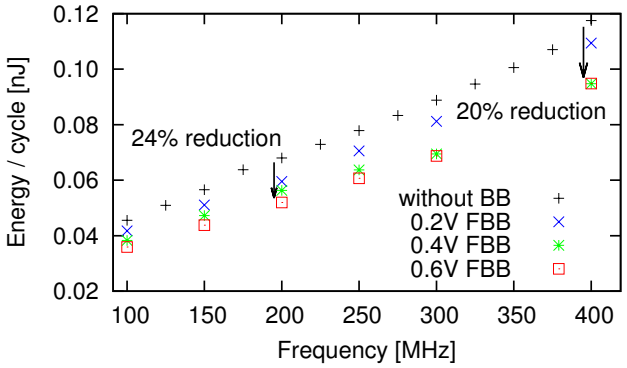

Fig. 13. Energy per cycle versus operating frequency with and without body bias tuning.

reduction. Whereas, keeping the threshold at a higher value is necessary for memory circuits. We have discussed on a system architecture where each circuit block will be body biased independently so that the optimum energy profile can be achieved. On-chip monitors are used to achieve the target device threshold characteristic and also to compensate temperature and process variation. The use of on-chip monitors as a link between device and circuit, and using them to control device characteristics according to circuit architecture by means of body biasing, large amount of energy reduction is possible. The above architecture also minimizes the margins required for PVT variations, thus design time optimization can be improved further. Our proposed concept is verified by demonstrating measurement results from two proof-of-concept circuits implemented in a 65 nm process. There are several issues that need to be solved for the wide adoption of the above concept. First, the EDA design flow need to adopt design automation of partitioning the design into several "substrate islands". Second, automatic placement of monitors and parameterized adoption of body bias generators are also required for low-cost and area-efficient implementation. We look forward to the development of such design time optimization techniques along with robust test strategy.

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