Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp132-133

Area-efficient Reconfigurable Ring Oscillator for Characterization of Static and Dynamic Variations

A.K.M Mahfuzul Islam*, and Hidetoshi Onodera*†
* Graduate School of Informatics, Kyoto University, Kyoto, Japan
† JST, CREST
email: {mahfuz,onodera}@vlsi.kuee.kyoto-u.ac.jp

I. Introduction

With device scaling, not only static device variability but also dynamic variations as random telegraph noise (RTN) has become serious threats [1–3]. Accurate characterization and modeling of these variations are needed for design margin setting and reliable operation.

In order to measure the statistical properties of static variations as within-die (WID) and dynamic variations as RTN, large number of samples are required. Conventionally, device-array based test structure [4], [5], or ring oscillator (RO) array based test structures [6] are used. RO based approach gives us the information of devices under switching conditions which represent the digital circuits. However, RO based measurement does not give us the information on the underlying variations. Various approaches are proposed to make the RO frequency sensitive to a particular variation source [7–9]. In order to characterize transistor-by-transistor variability, an inhomogeneous structure is proposed [10] which makes the RO frequency sensitive to a small set of transistors. The existing techniques have two fundamental problems. One is the large area required for large samples. The other is the inability of device identifications for accurate characterization and modeling. In order to overcome these problems, we propose a reconfigurable RO structure. With a single proposed RO, large samples can be measured with device identification.

II. Reconfigurable Ring Oscillator

Fig. 1 shows our proposed reconfigurable RO structure where reconfigurable inverter cells are used. Each cell can be configured to several delay modes ((a)–(d)). The sensitivity of a particular stage's delay is enhanced by configuring the RO as an inhomogeneous structure [10]. For nMOSFET characterization, Fig. 1(b) configuration is used for a particular stage, and Fig. 1(a) for all other stages. This configuration makes the RO frequency sensitive to the nMOSFETs of the inhomogeneous stage only. In order to identify the devices, we place two pass-gates in parallel as in Fig. 1 (C2 and C3, C4 and C5). With this structure, device mismatch can be measured directly by taking the difference between the frequencies by turning one of the two parallel pass-gates ON and other OFF, and vice versa. To identify devices with RTN effects, frequency fluctuation is observed for each pass-gate configuration. Thus, device level characterization becomes possible under switching condition. With an N-staged RO, N types of inhomogeneous configurations for either nMOSFET or pMOSFET can be sampled. Thus, statistical properties can be obtained by choosing N to be sufficient large. Die-to-die (D2D) variation and location correlated variations are measured by configuring the RO as homogeneous [9].

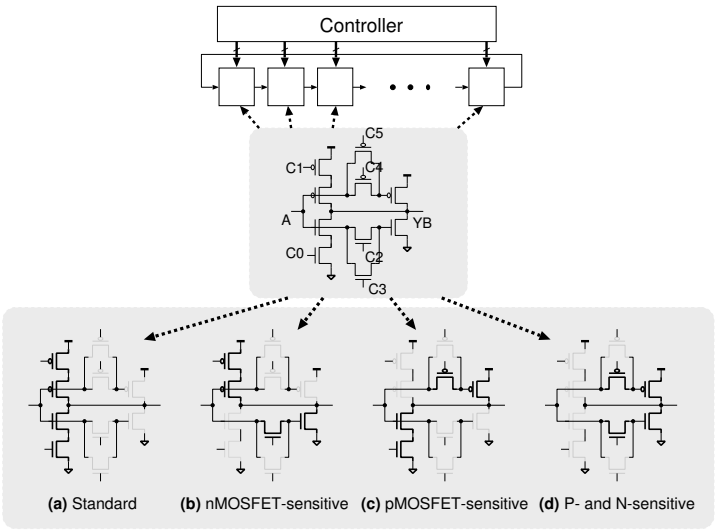


Fig. 1: Proposed Reconfigurable ring oscillator (RO) with reconfigurable inverter cells. Each inverter cell can have delay configuration of (a) standard, (b) nMOSFET-sensitive, (c) pMOSFET-sensitive, or (d) both nMOSFET- and pMOSFET-sensitive.

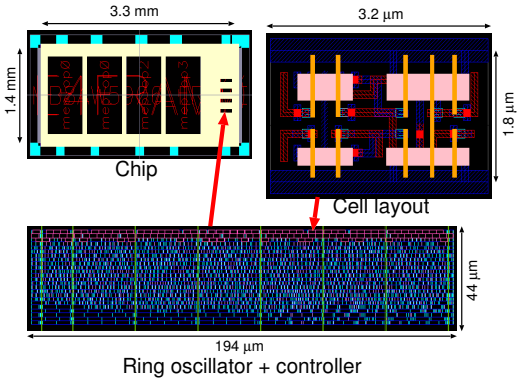
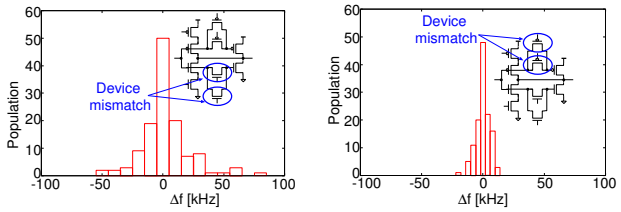


Fig. 2: Layout example of our proposed reconfigurable RO structure. Standard cell based design flow is used.

III. Test Chip Design and Measurement Results

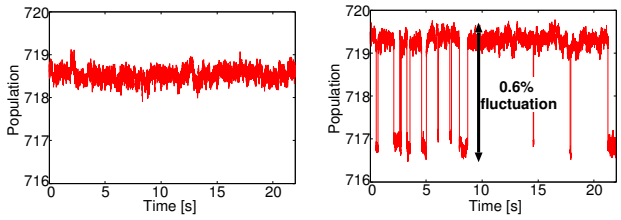
A. Test Chip Design

A test chip is fabricated in a 65-nm process to validate our proposed structure. Fig. 2 shows the chip floorplan along with the layout of the reconfigurable inverter cell, the RO, and the controller. The inverter cell has the same height as of the standard cells to allow conventional cell based design. This approach reduces implementation and design cost. The proposed ring oscillator thus can be embedded in any digital



(a) nMOSFET (b) pMOSFET

Fig. 3: WID device variations at 0.8 V supply.



(a) C2: ON, C3: OFF. (b) C2: OFF, C3: ON.

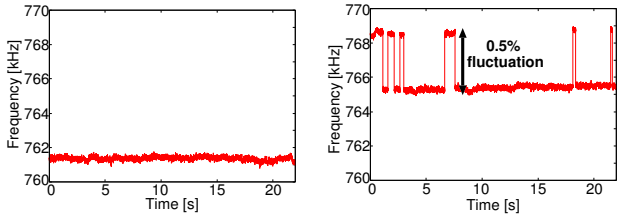
Fig. 4: Frequency fluctuation over time when C2 and C3 nMOSFET pass-gates of the inhomogeneous stage are turned on alternately.

circuit. The RO is 127-staged. The area of our proposed RO with the controller is 0.0085 mm^2.

B. Measurement Results

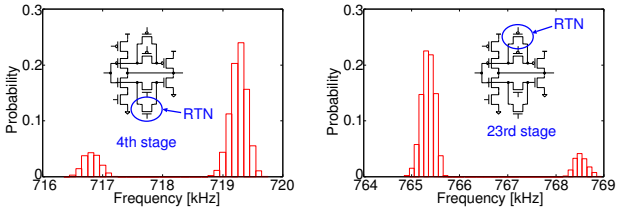
1) WID Variation: Fig. 3(a) shows the histogram of frequency differences when C2 and C3 pass-gates (nMOSFET pass-gates) are ON alternately. The frequency difference is the function of the device mismatch between these two transistors. Thus, device mismatch is directly measured with our proposed structure. Fig. 3(b) shows the histogram when C4 and C5 pass-gates (pMOSFET pass-gates) are ON alternately. Both the distributions are Gaussian suggesting we could measure the random variation. nMOSFET variability is measured to be larger than that of pMOSFET which agrees with the results reported in [5]. These variations can be further analyze to extract underlying variation sources with the methods presented in [9], [10].

2) RTN: In order to measure RTN effects, RO frequency for each inhomogeneous configuration is measured for 22 s with an integration time of 1 ms. For each configuration the pass-gate configuration is swapped to identify devices with RTN. In this test chip, We could find several samples



(a) C4: ON, C5: OFF. (b) C4: OFF, C5: ON.

Fig. 5: Frequency fluctuation over time when C4 and C5 pMOSFET pass-gates of the inhomogeneous stage are turned on alternately.



(a) nMOSFET (b) pMOSFET

Fig. 6: Frequency histogram for Figs. 4(a) and 4(b). Binary fluctuation is observed when C3 pass-gate is turned on meaning C3 pass-gate is RTN affected only.

with RTN effects. Figs. 4(a) and 4(b) show frequency fluctuations over time (22 ms) for an nMOSFET-sensitive inhomogeneous configuration. Fig. 4(a) shows the frequency fluctuation when the C2 pass-gate in Fig. 1 is turned ON and C3 pass-gate is turned OFF. Fig. 4(b) shows the frequency fluctuation for an apposite configuration (C2 OFF and C3 ON). C2 pass-gate ON configuration shows no binary fluctuation whereas C3 pass-gate ON configuration shows binary fluctuation which indicates that C3 pass-gate is RTN affected. Figs. 5(a) and 5(b) show two examples for pMOSFET RTN effects. RTN is observed when C4 transistor is turned OFF and C5 transistor is turned ON referring that C5 transistor is RTN affected. Thus, by changing the configuration we can identify each transistor's characteristic.

IV. Conclusion

An area-efficient reconfigurable RO structure is proposed for accurate characterization of device level static and dynamic variations. Measurement results from a 65-nm test chip confirms the validity of the proposed structure.

References

[1] M. Kirton and M. Uren, "Noise in solid-state microstructures: a new perspective on individual defects, interface states, and low-frequency noise," *Advances in Physics*, vol. 38, no. 4, pp. 367–468, 1989.

[2] K. Takeuchi, et al., "Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment," *Symposium on VLSI Technology*, pp. 189–190, Jun. 2010.

[3] N. Tega, H. Miki, and F. Pagette, "Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm," in *Symposium on VLSI Technology*, 2009, pp. 50–51.

[4] K. Agarwal, J. Hayes, and S. Nassif, "Fast Characterization of Threshold Voltage Fluctuation in MOS Devices," *IEEE Trans. on Semiconductor Manufacturing*, vol. 21, no. 4, pp. 526–533, Nov. 2008.

[5] T. Tsunomura, et al., "Analyses of 5σ Vth fluctuation in 65nm-MOSFETs using takeuchi plot," in *Symposium on VLSI Technology*, 2008, pp. 156–157.

[6] H. Onodera and H. Terada, "Characterization of WID delay variability using RO-array test structures," in *IEEE 8th International Conference on ASIC*, Oct. 2009, pp. 658–661.

[7] M. Bhushan, et al., "Ring oscillators for CMOS process tuning and variability control," *IEEE Trans. on Semiconductor Manufacturing*, vol. 19, no. 1, pp. 10–18, 2006.

[8] M. Bhushan, et al., "Ring oscillator based technique for measuring variability statistics," in *IEEE Intl. Conf. on Microelectronic Test Structures*, Mar. 2006, pp. 87–92.

[9] A. Islam, et al., "Variation-sensitive Monitor Circuits for Estimation of Global Process Parameter Variation," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 4, pp. 571–580, 2012.

[10] S. Fujimoto, et al., "Inhomogeneous Ring Oscillator for WID Variability and RTN Characterization," in *IEEE Intl. Conf. on Microelectronic Test Structures*, 2012, pp. 25–30.