A Body Bias Generator with Wide Supply-Range down to Threshold Voltage for Within-Die Variability Compensation

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***Abstract*—A body bias generator (BBG) for fine-grain body biasing (FGBB) that can operate under wide supply-range is proposed. While FGBB is effective in reducing variability and power consumption, a number of BBGs are required on a die and therefore simplified design of BBGs is necessary. This paper proposes a cell-based design of a BBG that generates forward and reverse body bias voltages only from a core supply voltage ranging from the near threshold of $500\mathrm{mV}$ to the nominal voltage of $1.2\mathrm{V}$. This wide operating range is achieved by a low voltage error amplifier with a V_{th} biasing scheme achieved by internal switched-capacitor charge pumping. We fabricated the forward/reverse BBG in a $65\mathrm{nm}$ low power CMOS process to control $0.22\mathrm{mm}^2$ of core circuit with the area overhead of 2.3% for the BBG.**

I. Introduction

Variability compensation on LSI is one of the emerging technologies. Though low supply voltage is important to reduce dynamic power of a system-on-chip (SoC), variability prevents lowering supply voltage.

It is also required to tune performance within a chip. The variability is classified into die-to-die and within-die variability. For example, location correlated within-die variability was measured in an 80-core processor [1]. They report that a maximum operating speed of each core were measured on a real chip and its spread was 62% at $V_{\mathrm{DD}} = 0.8\mathrm{V}$ between the fastest and the slowest cores on the die.

Fig. 1 (a) shows a concept of a fine-grain body bias (FGBB) to compensate within-die variability. Each grain is called "substrate island" in this paper. We assume that an SoC is partitioned into substrate islands and each substrate island has a body bias generator (BBG). It has been reported that the body bias achieved delay reduction and compensated die-to-die variability [2]. It showed that the body bias is an important technique to compensate the variability. Theoretical study for dynamic FGBB was also discussed [3], where dynamic FGBB was estimated to increase performance by 7–16% compared to zero body bias. It was also shown that FGBB improves minimum voltage of dynamic voltage frequency scaling.

For FGBB, the BBG should have precise resolution and small area and power overhead. In the reference [4], they measured operating frequency and leakage current under body bias and reported that resolution should be less than $100\mathrm{mV}$ to match their frequency and leakage constraints. Furthermore, preferable features are

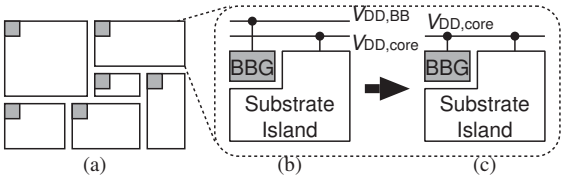

Fig. 1. (a) fine-grain body bias, (b) conventional body bias generator, and (c) concept of the low supply voltage body bias generator

1) Single supply voltage with a wide operating range: Extra supply voltage for BBG increases cost. The BBG should operate on the same supply lines with digital circuits where the supply voltage takes a wide range down to threshold voltage (V_{th}) of MOSFETs.
2) Wider output voltage: To compensate within-die variability, the BBG output voltage should be wide enough. In case that location correlated variability in threshold voltage is at most $50\mathrm{mV}$ and backgate transconductance is one-fifth of the transconductance, output voltage range should be at least $250\mathrm{mV}$ to compensate the variability. In addition, it is preferred to output both forward body bias (FBB) and reverse body bias (RBB); FBB for timing enhancement and RBB for leakage current reduction.
3) Automated design: Since a number of substrate islands exist in one chip, design cost of BBGs should be low enough.

In this paper, we propose a BBG with a wide range of supply voltage, which is able to operate down to threshold voltage from nominal supply voltage. The proposed BBG has two advantages. First, minimum supply voltage is reduced from our previous work [5] by improving amplifier topology and its peripheral circuits. Second, without requiring additional power/ground rails, the output voltage range goes beyond that of the supply for reverse body bias (RBB).

The remaining of this paper is organized as followings. In section II, we describe about supply voltage requirements for the BBG and discuss our proposal to satisfy it. In section III, we describe detailed implementation of the BBG. In section IV, we show measured results of the BBG, and conclude in section V.

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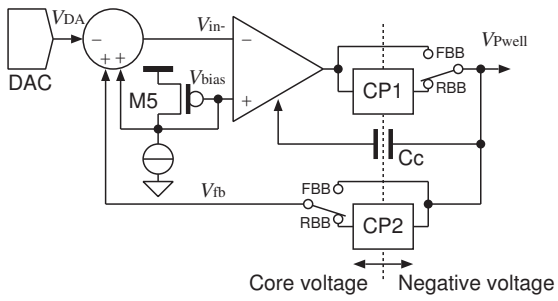


Fig. 2. The BBG with wide supply voltage range.

II. Key features of the proposed BBG

As mentioned in Section I, there are two difficulties toward our goal. This section describes our solution for single supply voltage operation and wide output voltage.

A. Voltage isolation by switched capacitor

As described in the previous section, every block of the BBG have to output both forward- and reverse- body bias with core supply voltage.

When biasing NMOSFET on P-well, RBB means negative voltage less than VSS. In contrast, when biasing PMOSFET on N-well, RBB means high voltage larger than VDD. In simplicity of discussion below, we describe BBG biasing NMOSFET.

Our solution to generate RBB is to isolate core voltage region and negative voltage region as described in Fig. 2. Charge pumps (CP1 and CP2) and phase compensation capacitor (Cc) bridge two regions and they are designed not to exceed voltage limitation of core devices. In the core voltage region, there are DAC, subtractor, and amplifier. Each block operates with core supply voltage.

B. Amplifier with $V_{\rm th}$ biasing input

The amplifier is also required to operate with wide supply voltage range down to near threshold voltage ($V_{\rm th}$).

For near threshold voltage operation, one input node of the amplifier is biased with diode-connected MOSFET and tail current source is eliminated as shown in Fig. 3. In our previous work [6], we proposed a method to reduce supply voltage by biasing constant voltage to one input node of the amplifier shown in Fig. 3 (a). But it was difficult to determine bias voltage at low supply voltage.

As shown in Fig. 2, the bias current is determined by the diode-connected MOSFET (M5). This biasing enables all transistors operating in saturation region at any supply voltage higher than the threshold voltage. By this biasing technique, the amplifier topology shown in Fig. 3 (b) can be utilized and pushes the lower limit of the supply voltage down.

III. Implementation

This section describes details of circuit blocks in Fig. 2.

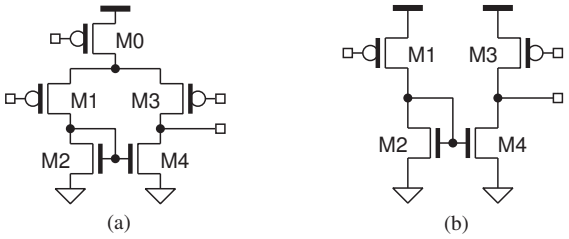


Fig. 3. Near threshold voltage amplifier design. (a) conventional differential to single-end amplifier. (b) Near threshold voltage amplifier with very narrow input swing.

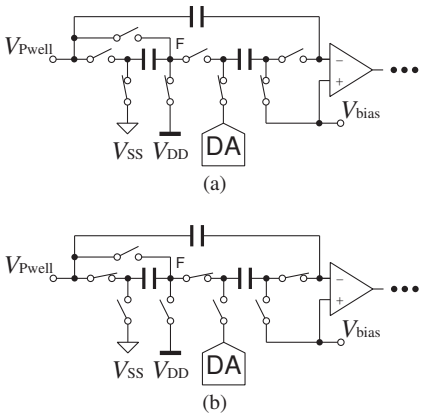


Fig. 4. Feedback charge pump phases; (a) biasing phase and the DAC is at the end of conversion, (b) amplification phase and the DAC is in conversion.

A. DAC

The proposed BBG has a serial charge redistribution DAC.

A resolution of the DAC is 6-bit, which is determined by the timing generator. The resolution is $19\mathrm{m}\mathrm{V}$ in $1.2\mathrm{V}$ supply voltage, which is equivalent to $4\mathrm{m}\mathrm{V}$ in the threshold voltage of a transistor in the substrate island.

B. Output charge pump for reverse body bias driving

If the RBB is requested, CP1 in Fig. 2 generates negative voltage. Output voltage of the amplifier is shifted to negative voltage by a capacitor.

To acquire enough current to drive load without large area penalty, we utilize high frequency clock to drive CP1. Metal-fringe capacitor of lower fine layer and bulk-gate capacitor were utilized for capacitors in CP1.

C. Feedback charge pump as accurate voltage level shifter

While output is reverse body bias (RBB), it is required to feedback negative voltage to the amplifier. A charge pump CP2 in Fig. 2 operates as a voltage level shifter to feedback negative voltage into core voltage region.

For enough linearity between FBB and RBB, voltage accuracy of the charge pump is important. This point is different from the charge pump CP1. We consider switching frequency and capacitor layout.

At low supply voltage, on-resistance of switch become large and it slow to charge the capacitor. The switching frequency should be reduced enough to finish charging in a cycle.

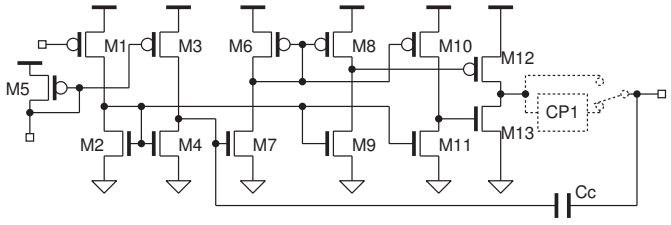


Fig. 5. Schematic of the amplifier

On the other hand, subtractor requires voltage only at its amplification phase. We chose to synchronize every feedback circuits; DAC, subtractor, charge pump CP2 as shown in Fig. 4. when the DAC has finished conversion, the charge pump and the subtractor go biasing phase to charge capacitors to intended voltage. While the DAC is converting, the charge pump and the adder are in amplification phase to feedback the voltage.

The most critical point to the accuracy is parasitic capacitance on node `F` in Fig. 4. The layout of the capacitor was carefully designed to reduce parasitics on node `F`.

D. Amplifier for wide operating voltage range

Fig. 5 shows a schematic of the amplifier. Though the amplifier itself operates with core supply voltage, thanks to the charge pump CP1, output voltage range of the BBG includes RBB and FBB.

To reduce steady state power consumption in the BBG, a third stage is implemented as a class B rail-to-rail output. Gate widths of `M8–11` is designed to make a dead zone of class B operation. Detailed of the third stage is discussed in [6].

E. Phase compensation

The phase compensation capacitor (`Cc`) consists of a gate-drain-source connected MOSFET utilizing gate-body capacitance. In order to suppress noise from the charge pump, the capacitor `Cc` is not connected to amplifier output but connected to charge pump output.

To keep stability in any V_{DD}, bias current for the amplifier is kept constant. Desired bias current of the first stage ensures phase margin always larger than $45°$. We assume maximum load capacitance of $300\mathrm{pF}$ for P-well and $200\mathrm{pF}$ for N-well.

F. Layout

We designed and fabricated a test circuit of the BBG in a $65\mathrm{nm}$ low power CMOS process with triple well structure and dual V_{th}. The area of the core circuit to be controlled is $0.22\mathrm{mm}^2$ and the area of the BBG is $0.0052\mathrm{mm}^2$ and area overhead is 0.23%.

We designed the BBG compatible with cell-based CAD tools for digital designs. The cell-based design strategy was explained in [5].

Fig. 6 shows the result of the placement and fabricated chip photograph. We integrated a process monitor [7], [8] and an AES cipher core.

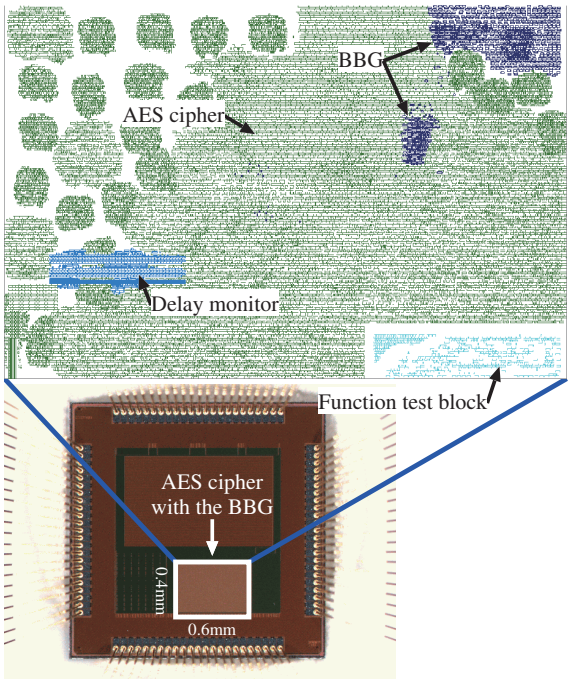
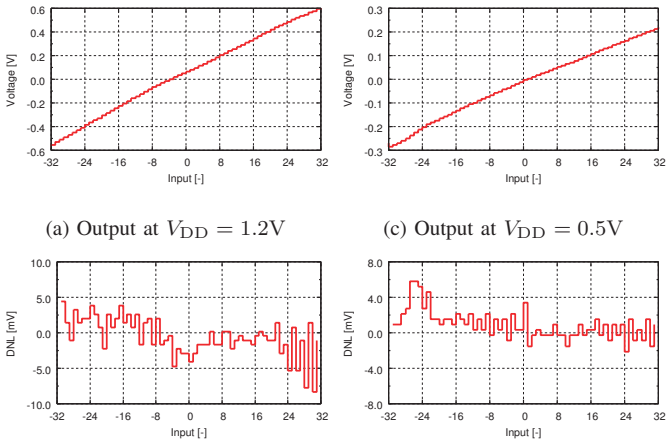


Fig. 6. Chip photograph and placement of the BBG



(a) Output at $V_{\mathrm{DD}} = 1.2\mathrm{V}$ (c) Output at $V_{\mathrm{DD}} = 0.5\mathrm{V}$

(b) DNL at $V_{\mathrm{DD}} = 1.2\mathrm{V}$ (d) DNL at $V_{\mathrm{DD}} = 0.5\mathrm{V}$

Fig. 7. Measured output voltage and DNL from reverse body bias to forward body bias.

IV. Measured Results

Fig. 7 shows output voltage and differential nonlinearity (DNL) for each input code at (a, b) $V_{\mathrm{DD}} = 1.2\mathrm{V}$ and (c, d) $V_{\mathrm{DD}} = 500\mathrm{mV}$. The DNL is less than 0.5 LSB, which is small enough for the purpose of variability compensation and SoC power reduction.

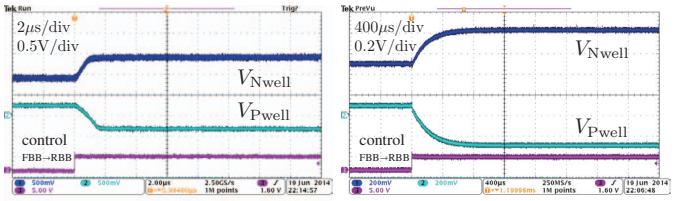
Transient responses were also measured to confirm stability of the feedback loop. Fig. 8 (a) shows transient response from FBB to RBB at $V_{\mathrm{DD}} = 0.5\mathrm{V}, f = 2.5\mathrm{MHz}$. Fig. 8 (b) shows transient response from FBB to RBB at $V_{\mathrm{DD}} = 1.2\mathrm{V}, f = 250\mathrm{MHz}$. Every step has no dumping.

Table I shows the performance comparison of the BBG. The

Table I
SUMMARY AND PERFORMANCE OF THE BBG.

Parameter	this work	prev. work [5], [6]	[9]	[10]	[2]
Process	65nm	65nm	90nm	90nm	65nm
Supply	**500mV to 1.2V**	0.6V to 1.2V	1.2V	2.5V & −1V	> 1.1V
Core supply	500mV to 1.2V	0.6V to 1.2V	0.8V to 1.2V	1.0V	1.2V
Output	FBB/RBB	FBB	FBB	FBB/RBB	FBB
Resolution	19mV †	38mV	8mV	-	binary
BBG circuit area	0.0052mm^2	0.0023mm^2	0.03mm^2	0.006mm^2	-
Core circuit area	0.22mm^2	0.1mm^2	1mm^2	0.15mm^2	15mm^2
Area overhead	2.3%	2.3%	3%	4%	< 3%
Layout design	automated	automated	modular	custom	automated
Power consumption	0.6mW	0.12mW	0.21mW	1.5mW	-
Response time	2μs ‡	2μs	5μs	70ns	-

† is a maximum value at $V_{\text{DD}} = 1.2\text{V}$ and is proportional to V_{DD}.
‡ is at $V_{\text{DD}} = 1.2\text{V}$ and it also depends on input values.



(a) (b)

Fig. 8. Measured transient response, (a) $V_{\text{DD}} = 1.2\text{V}$, (b) $V_{\text{DD}} = 500\text{mV}$.

proposed forward/reverse BBG has a wide range of supply voltage from 500mV to 1.2V.

Power consumption of the BBG is 0.6mW and that of the AES cipher is larger than 12mW at $V_{\text{DD}} = 1.2\text{V}$. Power overhead of the BBG is less than 5%.

V. CONCLUSION

In this paper, we present a forward/reverse BBG. The proposed BBG was fabricated in a 65nm CMOS process with dual threshold voltages. The BBG design achieves small area overhead of 2.3% and power overhead less than 5%. The lab evaluation proofed that the BBG operates wide range of supply voltage from 500mV to 1.2V and are suited for low power SoC application.

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