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On-chip leakage current variation measurement using external-reference-free current-to-time conversion for densely placed MOSFETs

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This paper proposes a time-domain leakage current measurement circuit that uses an external-reference-free current-to-time conversion. Our proposed current-to-time converter (CTC) utilizes a dual inverter-based conversion to provide a stable reference. We share the CTC among the devices under test (DUTs) for accurate characterization of variation. Our CTC, along with a tree-based switch structure, allows us to densely place and route the DUT transistors using a cell-based design flow similar to a digital circuit design. We demonstrate our circuit by measuring subthreshold leakage currents of 256 minimum sized nMOSFETs in a 65 nm bulk low-power CMOS process. We could successfully extract the variations in subthreshold coefficient and subthreshold leakage current at different temperatures. Our circuit is also robust to supply voltage fluctuation making the circuit suitable for accurate characterization of MOSFET parameters for subthreshold operation.

1. Introduction

Accurate measurement of MOSFET leakage current and its variation is indispensable for statistical modeling and performance prediction especially for circuits operating at low supply voltage.[1–3] There are numerous reports of measurement circuits for characterizing leakage current and threshold voltage variations.[4–10] However, most of the measurements are performed in a device matrix where the devices are placed in a highly regular layout. The devices are often placed with low density compared to that found in a design performed with an automatic place and route design. In this paper, we propose a time-domain leakage current measurement circuit where the devices are placed and routed randomly with high density using the cell-based design flow. Furthermore, we use only thin oxide devices. Thus, the proposed design can be embedded anywhere in the chip.

To accurately measure leakage current across a wide temperature range, a stable reference voltage is typically required. Generating or providing a reference voltage increases design and fabrication costs. In the state-of-the-art time-domain leakage current measurement, analog comparators are mostly used.[11] Here, we propose a technique that utilizes the logical threshold voltage difference of two inverters instead of using a comparator with a reference. The use of inverters eliminates the need for analog comparators and reference voltages. We demonstrate that a threshold voltage difference provides a stable voltage reference that is constant over a wide range of temperatures.

There are time-domain leakage current variation measurement circuits that utilize a ring oscillator-based configuration.[12] In the case of a RO, inverter delays cause errors. To reduce the impact of inverter delays, the large capacitor is required at the output node. Therefore, it is not possible to realize the same dense layout for the DUTs. Furthermore, compared with an RO-based approach where the drain voltage suffers large fluctuation, our circuit measures the leakage current at a almost constant drain voltage. We then develop a tree-based switching scheme to reduce the number of parallel paths. We demonstrate our measurement circuit by measuring subthreshold leakage currents of 256 minimum sized transistors in a 65 nm bulk low-power CMOS process at different temperatures under different supply voltages. This paper is an extension of the conference paper presented at the International Conference on Solid State Devices and Materials.[13] Compared with the conference paper, we have added a detailed explanation of the design issues and operating principle of our measurement circuit. We have then added several variability characterization methodologies and presented variation results of subthreshold coefficient and threshold voltage.

The remainder of the paper is organized as follows. In Sect. 2, we describe the operating mechanism of our proposed circuit along with the measurement flow. We then describe some methodologies for extracting variations of subthreshold current, subthreshold coefficient and threshold voltage in Sect. 3. In Sect. 4, we describe our test chip and demonstrate the measurement results. Finally, we conclude the paper in Sect. 5.

2. Leakage current measurement circuit

2.1. Current-to-time converter

Figure 1 shows our proposed current-to-time converter. The capacitor C_L is first charged to V_{dd} by turning the M_{charge} ON. Then, C_L is discharged through a selected DUT MOSFET. The time interval d between the two outputs' switching transition is then measured. The discharge time d_{ia} from V_{dd} to V_{X1}, and the discharge time d_{ib} from V_{dd} to V_{X2} for the ith MOSFET can be approximated as follows.

$$d_{ia} \simeq \frac{(V_{dd} - V_{X1}) \cdot C_L}{I_i} + \varepsilon_a, \tag{1}$$

$$d_{ib} \simeq \frac{(V_{dd} - V_{X2}) \cdot C_L}{I_i} + \varepsilon_b. \tag{2}$$

Here, I_i is the drain current of the ith selected MOSFET M_i, and ε_a and ε_b are inverter delays. In a typical current to time conversion, inverter or comparator delay causes an error in the measurement. Here, as we measure the delay difference d_i corresponding to the ith DUT M_i with drain current I_i which can be expressed as follows.

$$d_i = d_{ib} - d_{ia} \simeq \frac{(V_{X1} - V_{X2}) \cdot C_L}{I_i} + (\varepsilon_a - \varepsilon_b). \tag{3}$$

For accurate measurement of subthreshold leakage current, we need to make sure that the following issues are properly addressed.

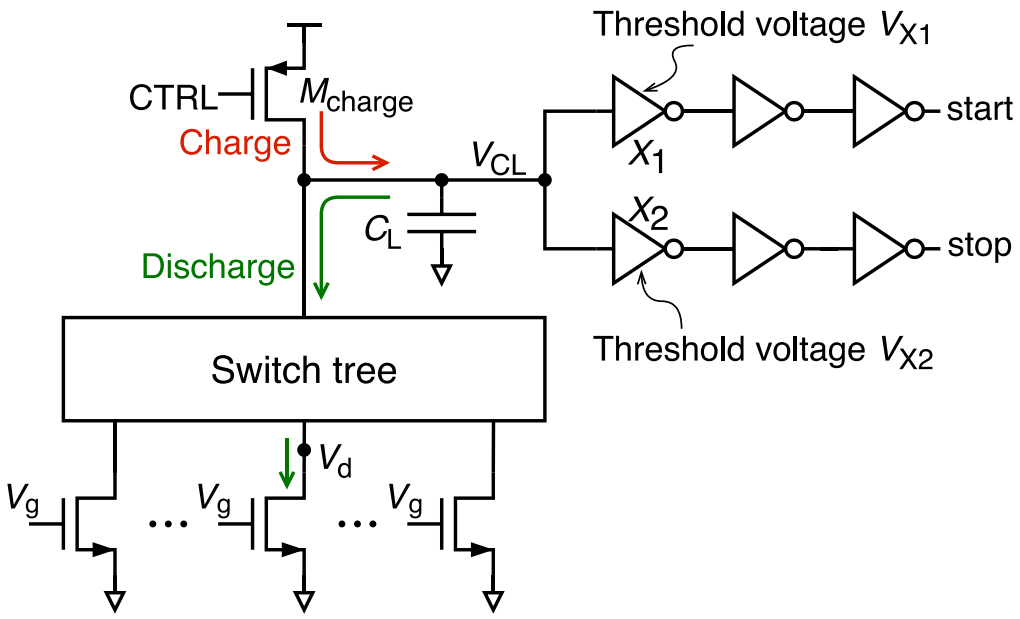


Fig. 1. (Color online) Topology of our proposed compact current-to-time converter.

(1) Cancel out the inverter delay,
(2) minimize the voltage drop across the switch tree,
(3) make $(V_{X1} - V_{X2})$ stable across a wide temperature range, and
(4) make V_{ds} fluctuation of the selected MOSFET small during the measurement.We explain the different design decisions to meet the above-mentioned requirements in the following. First, if we design the two inverters to have similar transition delay, the term $(\varepsilon_a - \varepsilon_b)$ becomes negligible. These delay components can be expressed as follows.

$$\varepsilon_a = \frac{C_{out1} \cdot V_{X1}}{I_{p1}}, \varepsilon_b = \frac{C_{out2} \cdot V_{X2}}{I_{p2}}. \tag{4}$$

$$\frac{\varepsilon_a}{\varepsilon_b} = \frac{C_{out1}}{C_{out2}} \cdot \frac{I_{p2}}{I_{p1}} \cdot \frac{V_{X1}}{V_{X2}}. \tag{5}$$

Here, C_{out1} and C_{out2} are output load capacitances for the two inverters. V_{X1} and V_{X2} are the logic threshold voltages. I_{p1} and I_{p2} are the driving currents. Based on Eq. (5), we can tune the load capacitance ratio such that $\varepsilon_a/\varepsilon_b$ is close to 1. The load capacitances can be adjusted by tuning the gate area of the following inverters. Thus, using a time-difference-based approach, the effects of inverter delay can be canceled out.

Second, we explain the minimization method of the switch resistance. As shown on the left side of Fig. 2, the gate-source voltage of the switch transistor is small during the initial period which may cause an error in the conversion. To reduce the effect of the switch transistor's resistance, the drain voltage of the switch should be low enough. As the right side of Fig. 2 shows, the voltage drop across the ON-state switch is not negligible when V_d is high. After the drain voltage V_d, which corresponds to the output node voltage, is sufficiently low, the voltage drop across the switch becomes negligible. Thus, the voltage drop across the switch tree can be minimized by making sure that the measurement is taken when the output node voltage is sufficiently low such that the voltage drop across the switches is close to zero. In the figure, when capacitor node voltage V_{CL} reaches V_{X1}, which is 0.38 V in this design at 1.0 V operation, V_{CL} and internal node voltage V_d are almost identical.

Third, as the same types of pMOSFET and nMOSFET are used for the inverters, both of the inverter logic threshold voltages are expected to have similar temperature coefficients. Logic threshold voltage V_X of an inverter can be expressed as follows.[14)]

$$V_X = \frac{V_{dd} + V_{thp} + \sqrt{\gamma} V_{thn}}{1 + \sqrt{\gamma}}, \tag{6}$$

$$\gamma = \frac{\mu_n C_{oxn} W_n / L_n}{\mu_p C_{oxp} W_p / L_p}. \tag{7}$$

Here V_{thp} and V_{thn} are threshold voltages of pMOSFET and nMOSFET, respectively. μ_p and μ_n represent mobility for pMOSFET and nMOSFET. C_{oxp} and C_{oxn} are gate oxide capacitances per area. W_p and W_n are the gate widths, and L_p and L_n are the gate lengths. γ here thus represents the driving strength ratio between nMOSFET and pMOSFET. From Eq. (6), we can tune the logic threshold by tuning γ and threshold voltages. Consider the case of tuning the logic threshold by adjusting the pMOSFET threshold voltages of the two inverters. In this case, ΔV_X is equal to $V_{thp2} - V_{thp1}$. Different threshold voltages can be obtained by gate length modulation for example. Threshold voltage typically has a sensitivity of 1–2 mV K^{-1} against temperature.[14)] Assuming both the threshold voltages change by the same amount with a change in temperature, we expect a stable ΔV_X over a wide range of temperatures. It should be noted that there are second-order dependencies that may cause some deviation. Figure 3 shows the simulated threshold voltage difference against temperature. The amount of fluctuation for $(V_{X1} - V_{X2})$ across a temperature range of 100 °C under five different process corners of "TT", "SF", "FS", "SS" and "FF" is plotted in the figure. We observe negligible fluctuation of $(V_{X1} - V_{X2})$ across the temperature range. Thus, we find the second-order effects to be small in the target process.

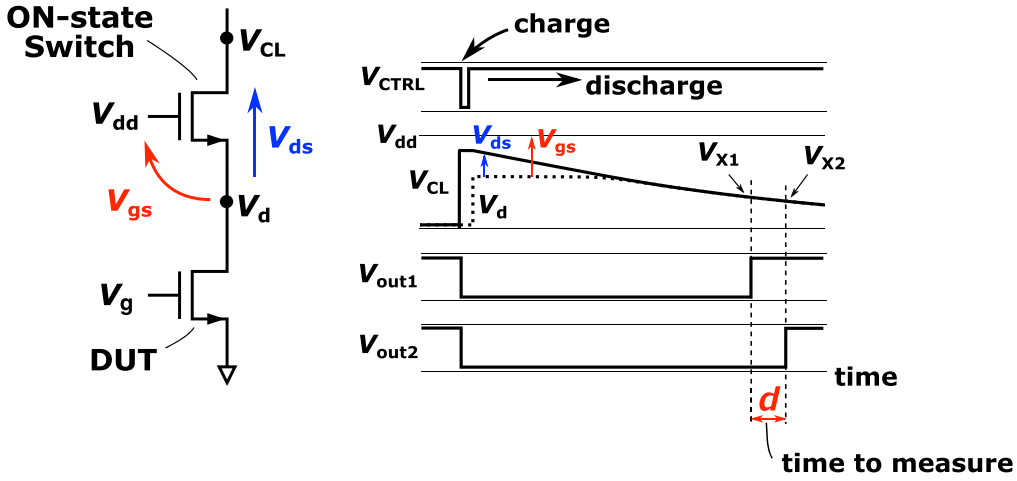


Fig. 2. (Color online) The ON-state switch transistor in the MOSFET selection circuit (left) and voltage waveform of current-to-time converter (right).

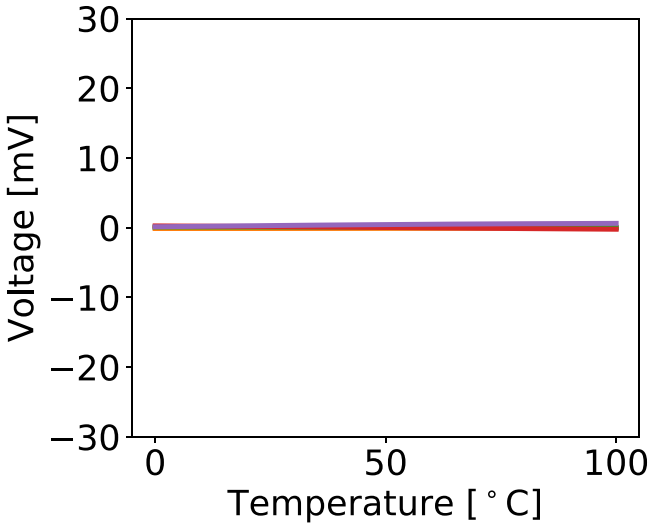


Fig. 3. (Color online) Deviation of logic threshold different at different temperatures and different process corners.

Finally, we also need to make sure that the drain voltage remains constant during the current measurement for accurate characterization of different process parameters such as the subthreshold coefficient and threshold voltage. This can be achieved by setting the two threshold voltages close to each other. As illustrated in Fig. 2, the inverters are designed such that the two threshold voltages of V_{X1} and V_{X2} become close to each other and these values are much lower.

2.2. Switch structure

The design of the switch tree is important to maximize DUT current ratio to other leakage current ratios. Putting all the DUT MOSFETs in parallel will cause large gate leakage which can be large in scaled processes. To reduce the number of parallel MOSFETs, we use a tree-based switch structure as shown in Fig. 4. In the structure, the switches are divided into several stages and each stage has several branches. With the stacking of the switches, the source voltage of the intermediate transistors rises resulting in negative V_{gs} and V_{bs} values. Negative V_{gs} and V_{bs} decrease the leakage current further. For the case of 256 DUT MOSFETs, the ratio between DUT current and other leakage currents is simulated to be 168 for the target process when $V_g = 0.2$ V.

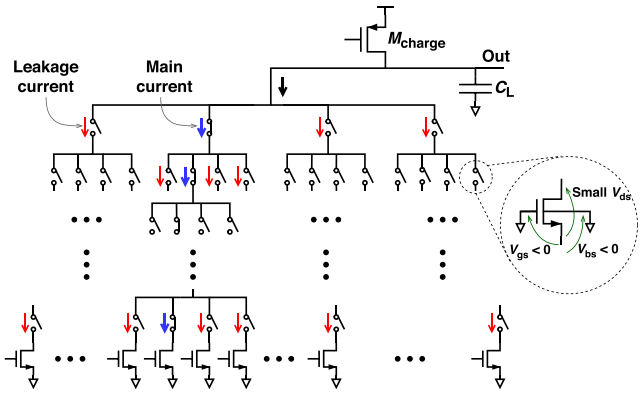


Fig. 4. (Color online) Tree structure of switches to reduce unwanted leakage current.

2.3. Overall architecture

Figure 5 shows the block diagram of our measurement circuit. Inside the chip, N number of DUT (Device Under Test) MOSFETs are placed and routed along with the switches. First, using serial clock "sclk" and serial data "sdin", the address of the target MOSFET is sent to the chip. The decoder inside the chip decodes the address and generates the signals for the switches to activate the path for the target MOSFET. The "meas" signal is then lowered for some time to allow the output node to charge to V_{dd}. The "meas" signal is then set to high to let the output node to be discharged by one of the DUT MOSFETs. After the output node is lowered to cross the logic threshold voltages of the inverters, the output signals "out1" and "out2" are then inverted sequentially. The delay difference between the two

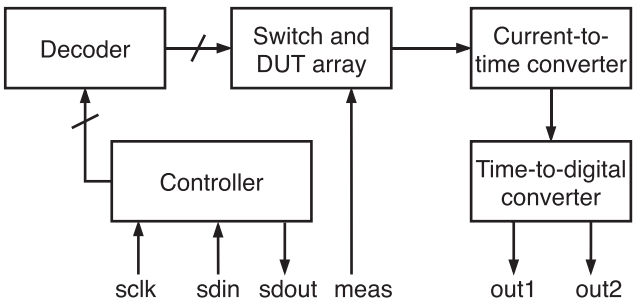


Fig. 5. Block diagram of proposed current measurement flow.

output signals gives the delay corresponding to the subthreshold current of the target MOSFET. This process is then iterated by selecting the next MOSFET.

A similar complementary test structure can be implemented to measure variations of pMOSFETs. In that case, the output node will be discharged to V_{ss} first, and then the node will be charged by one of the pMOSFETs. In this implementation, we change the address after the completion of each measurement by sending the serial signals which cause some delay. To reduce the test time further, we can implement a counter-on-chip that will increment the address value after the completion of each measurement.

3. Variability characterization methodology

3.1. Subthreshold leakage current

As $(V_{X1} - V_{X2})$ is shared among all the DUT devices, and its value is constant across temperature, we can relate the variance of delay to the variance of subthreshold leakage current as follows

$$\ln d = \ln(V_{X1} - V_{X2}) + \ln C_L - \ln I, \tag{8}$$

$$\mathrm{Var}(\ln d) = \mathrm{Var}(\ln I). \tag{9}$$

3.2. Subthreshold coefficient

The subthreshold coefficient of each MOSFET can be calculated by measuring the current at different gate-source voltages where the MOSFETs operate at weak inversion. Different gate-source voltages can be achieved by tuning V_g in our circuit. Choosing two values of V_g to be V_{g1} and V_{g2}, we obtain the following relationships.[15)]

$$I_1 = I_S \exp\left(\frac{V_{g1} - V_{th}}{mkT/q}\right), \tag{10}$$

$$I_2 = I_S \exp\left(\frac{V_{g2} - V_{th}}{mkT/q}\right), \tag{11}$$

$$d_2 = \frac{C_L(V_{X1} - V_{X2})}{I_2},\ d_1 = \frac{C_L(V_{X1} - V_{X2})}{I_1}, \tag{12}$$

$$\frac{d_2}{d_1} = \frac{I_1}{I_2}, \tag{13}$$

$$\ln\left(\frac{d_2}{d_1}\right) = \frac{q(V_{g2} - V_{g1})}{kT} \cdot \frac{1}{m}, \tag{14}$$

$$m = \frac{q(V_{g2} - V_{g1})}{kT} \cdot \frac{1}{\ln\left(\frac{d_2}{d_1}\right)}. \tag{15}$$

Here, I_S is the reverse saturation current, q is the elementary charge, k is the Boltzmann constant, m is the subthreshold coefficient, and T is the absolute temperature. From Eq. (15), we can obtain the value of subthreshold coefficient m for each MOSFET by measuring two delays at two different V_g values.

3.3. Threshold voltage

Accurate characterization of MOSFET threshold voltage variation is not straightforward. Different approaches are used in the literature to define threshold voltage to characterize its variation.[16–19)] We can see from Eq. (10) that the threshold voltage V_{th} and the subthreshold voltage m are closely coupled. These two values cannot be decoupled by tuning the V_{gs} values only. Thus, for scaled MOSFETs, where the subthreshold coefficient m varies largely, careful interpretation is required for threshold voltage variation. For larger devices, where m variation is negligible, V_{th} variation can be readily calculated by measuring delays at a constant V_g value using our circuit.[20)]

$$d = \frac{C_L(V_{X1} - V_{X2})}{I}, \tag{16}$$

$$\sigma_{\ln d} = \sigma_{\ln I} = \frac{\sigma_{V_{th}}}{mkT/q}, \tag{17}$$

$$\sigma_{V_{th}} = \sigma_{\ln d} \cdot \frac{mkT}{q}. \tag{18}$$

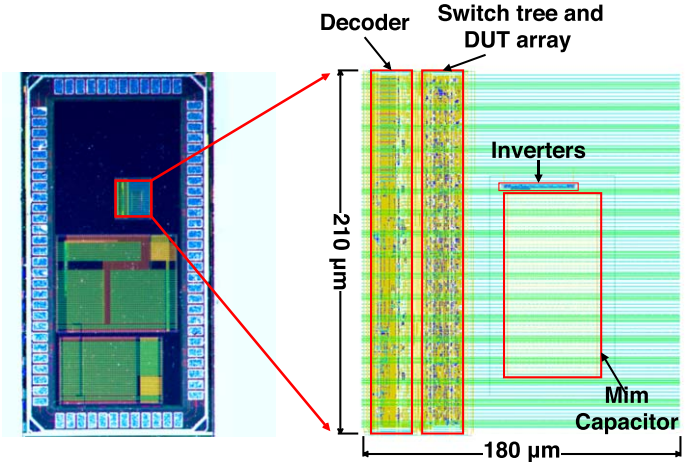


Fig. 6. (Color online) Chip photograph (left) and overall layout (right).

4. Measurement results

4.1. Test chip

We have fabricated a test chip integrating 256 nMOSFETs, the switch tree, the current-to-time converter, and the switch decoder in a 65 nm bulk low-power CMOS process. The layout is designed with a cell-based design flow. Figure 6 shows the chip photograph and layout of our proposed circuit. The area is 0.038 mm^2. C_L is implemented using MIM capacitor. The value of C_L is 10 pF in this test chip which takes an area of 0.0086 mm^2. The values of V_{X1} are 0.29 V, 0.38 V and 0.45 V at V_{dd} of 0.8 V, 1.0 V and 1.2 V, respectfully. The values of $V_{X1} - V_{X2}$ are 40 mV, 50 mV and 70 mV at the three supply voltages.

4.2. Subthreshold leakage current variation

Figure 7(a) shows the QQ plot of the logarithm of measured delays at $V_g = 0.2$ V for different temperatures. A linear relationship is observed referring to that leakage current follows a lognormal distribution. This is further confirmed by plotting the histograms of the logarithm of delays for two different temperatures of 0 °C and 100 °C. The histograms are shown in Fig. 7(b). We observe Gaussian-like histograms for the delay logarithms. The variance increases with the lowering of temperature. Figure 8 shows the standard deviation of logarithm of delay against $1/T$ for three different supply voltages. As predicted by Eq. (17), the standard deviation of the logarithm of delay has a linear relationship against $1/T$. We also observe the same linear relationship in Fig. 8, which confirms the validity of the measurement. We also observe that supply voltage change has negligible effect on the distribution.

4.3. Subthreshold coefficient variation

We have measured the delay value for each of the MOSFETs by measuring at different V_g values. Figure 9(a) shows the $1/d$ over a V_g range from 0.2 V to 0.4 V. We can observe that most of the devices show a linear relationship up to 0.3 V. However, some of the devices show nonlinear relation from 0.35 V which suggests that channel inversion has started for these devices at this point. Next, we have calculated the subthreshold coefficient

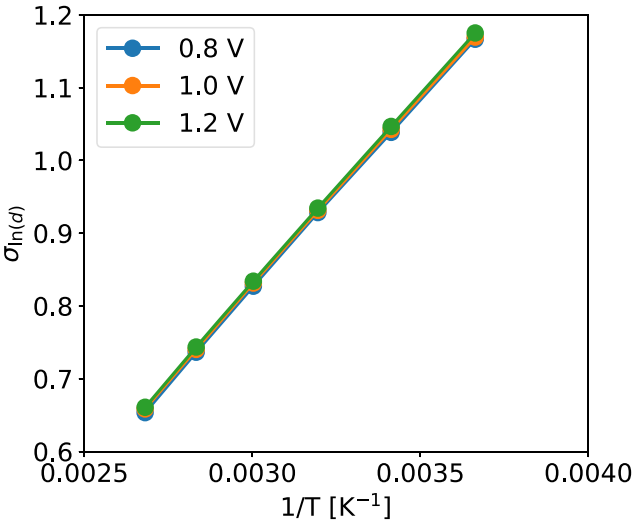
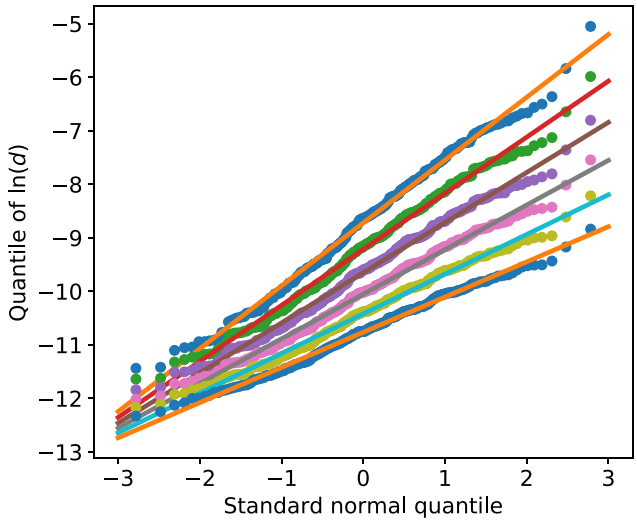


Fig. 8. (Color online) Standard deviation of the logarithm of measured delay against temperature for three different supply voltages of 0.8 V, 1.0 V and 1.2 V when $V_g = 0.2$ V.

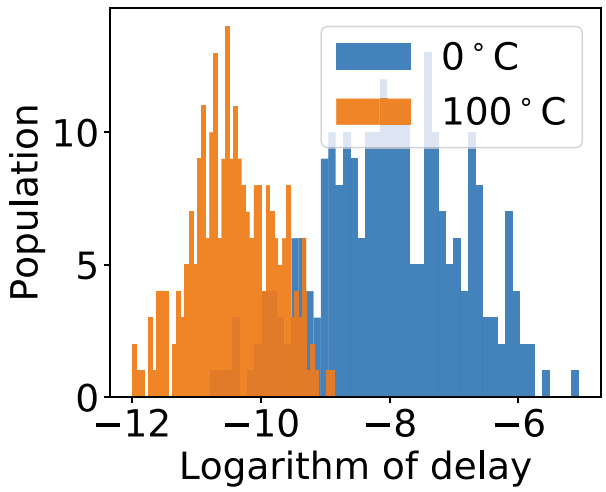
m for each of the nMOSFETs using delay values at V_g values of 0.2 V and 0.25 V. Figure 9(b) shows the histograms of the calculated m values for two different temperatures of 0 °C and 100 °C. We observe large variation in the m values. This observation is supported by literature reports.[21] However, to the best of our knowledge, our results are the first to demonstrate m distribution for scaled nMOSFETs that are densely placed as found in a digital circuit.

4.4. Threshold voltage

As seen in Fig. 9(b), subthreshold coefficient m is not constant in this process for the minimum sized nMOSFETs. Therefore, Eq. (18) cannot be applied. We need more sophisticated extraction methods to accurately extract threshold voltage variation. Understanding the limitation of Eq. (18), we derive V_{th} variation assuming that m is constant. We use the median value of m from Fig. 9(b). The extracted standard deviation of V_{th} is then calculated to be 37 mV at 20 °C temperature.

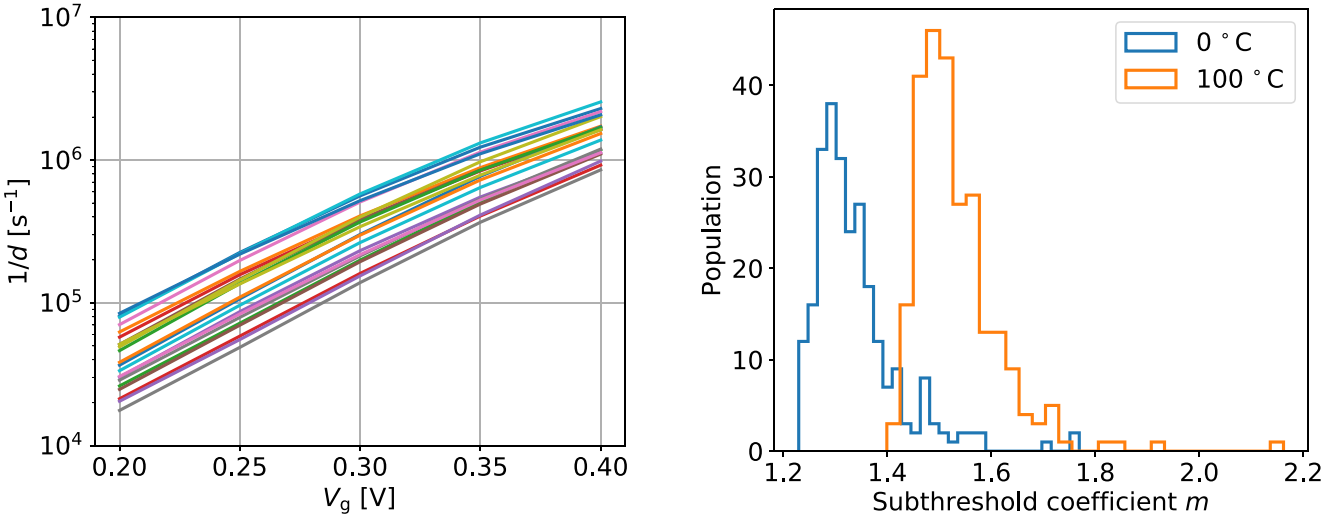


(a) QQ plots of logarithm of delays at different temperatures 0 °C, 20 °C, 40 °C, 60 °C, 80 °C and 100 °C when $V_g = 0.2$ V.



(b) Histogram of logarithm of delay.

Fig. 7. (Color online) Delay variability at different temperatures.



(a) $1/d$ versus V_g. (b) Histogram of m.

Fig. 9. (Color online) Variability of subthreshold coefficient m.

However, we should be careful that this value can be overestimated due to the variation in subthreshold coefficient m.

5. Conclusion

We proposed an on-chip leakage current measurement circuit for statistical modeling. The circuit shares a common current-to-time converter along with a tree-based switching scheme to reduce unwanted leakage currents. Furthermore, a dual interval-based current-to-time conversion reduces errors from comparator delay and switch resistances, as well as eliminates the need for external references. The proposed circuit will help the process engineers measure current variations at different temperatures and bias voltages under a cell-based design where the MOSFETs are densely placed and routed.

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