Low-Power Design of Digital LDO With Non-linear Symmetric Frequency Generation

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***Abstract*—This brief proposes a digital LDO (Low DropOut regulator) with a built-in non-linear VCO (Voltage Controlled Oscillator) to achieve both the fast transient response and low power operation. This on-chip VCO generates a clock signal whose frequency is a non-linear symmetric function of the output voltage error. Here, we propose a design technique to realize the symmetric frequency generation with low power consumption. We demonstrate a design example of LDO using our proposed technique in a commercial 65 nm low-power CMOS process. We evaluate the LDO using transistor-level simulation using HSPICE. It achieves 0.03-11 μA of quiescent current with an input voltage range of 0.6-1.2 V and an average current efficiency of 99.68 $\%$ across 50$\times$ load range.**

I. Introduction

Functional blocks are integrated into the same chip in modern electronic devices, making it a system-on-chip (SoC). Each block needs to operate at its optimum supply voltage to reduce the energy consumption of an SoC [1]. However, generating independent supply voltage for each block using DC/DC converters is not feasible. Therefore, on-chip LDOs (Low DropOut regulators) are often used to generate the required voltages. In such cases, the LDOs need to regulate the voltage for undershoot and overshoot.

Analog LDOs can regulate the output voltage for undershoot and overshoot [2], [3]. However, analog LDOs cannot operate at low supply voltage, which impedes energy optimization. Furthermore, analog LDOs require a large quiescent current, which is not suitable for low-power digital circuits. As an alternative, digital LDOs are gaining attention for their low supply voltage and wide load range operation [4]–[8].

Large output capacitors are not available for on-chip LDOs. Thus, power MOSFETs have to be controlled with a small delay when a fluctuation occurs to stabilize the output voltage. The output voltage must be sampled and processed with a high clock speed to achieve a small delay. High-speed processing and the generation of such clocks consume considerable power. Thus, a trade-off exists between the steady-state current and control delay in a typical digital LDO.

Adaptive tuning of clock frequency based on the output voltage error is essential to realize both low quiescent current and small control delay. To protect the output from both the undershoot and overshoot, symmetric frequency change is required against the voltage error. Several adaptive sampling techniques are proposed to realize this feature [9]–[12]. Refs. [9], [10] propose to choose between different clock signals depending on the output voltage error. The output voltage is monitored with three comparators with different reference voltages in this case. As the comparators need to operate under the higher speed clock, the power consumption becomes high in the steady-state operation. In Ref. [11], the sampling clock is generated from two clock signals generated by a VCO (Voltage Controlled Oscillators) pair. However, it is weak against random mismatches because it uses two different oscillators. Ref. [12] introduces an event-driven LDO which uses a 3-bit continuous-time ADC. The seven continuous-time comparators, in this case, consume large power.

This brief proposes an on-chip digital LDO with non-linear symmetric frequency generation to realize both the low quiescent current and fast transient response. The proposed VCO achieves a wide range of frequency tuning by a subthreshold current addition of a MOSFET pair driven by a differential error signal. Using a preamplifier and the differential operation ensures robustness against the process, voltage, and temperature variations without enlarging channel areas. A smaller channel area leads to a smaller node capacitance, resulting in high bandwidth with small current.

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II. Proposed LDO design

A. Operating principle

It is essential to tune the sampling frequency with a large range. Proposed LDO modulates the clock frequency non-linearly using the subthreshold current addition of a MOSFET pair. As shown in Fig. 1, the frequency of the generated clock is proportional to the current sum $I_{\rm p}+I_{\rm n}$. In order to modulate the clock frequency depending on the absolute error of the output voltage $|\Delta V_{\rm REG}| = |V_{\rm REG} - V_{\rm REF}|$, two MOSFETs which supply $I_{\rm p}$ and $I_{\rm n}$ are controlled by the differential output signals of a preamplifier. Here, $V_{\rm REF}$ is the reference voltage. If the pMOSFETs operate in the subthreshold region, drain current will change exponentially as shown below.

$$I_{\rm d} = I_{\rm s} \cdot \exp\left(\frac{V_{\rm IN} - V_{\rm g} - V_{\rm th}}{nV_{\rm T}}\right). \tag{1}$$

Here, $I_{\rm s}$, $V_{\rm g}$, $V_{\rm th}$, n, and $V_{\rm T}$ are reverse saturation current, gate voltage, absolute threshold voltage, subthreshold coefficient, and thermal voltage, respectively. Using the gain G of the preamplifier, the differential inputs of the MOSFET pair becomes $V_{\rm a\_p} = V_{\rm IN}/2 - G\Delta V_{\rm REG}$ and $V_{\rm a\_n} = V_{\rm IN}/2 +$

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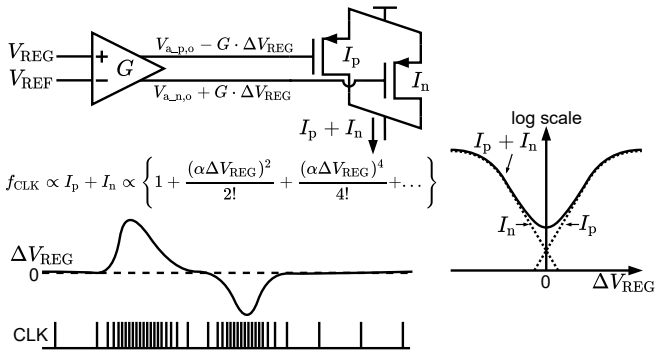

Fig. 1: Operating principle of non-linear frequency modulation ($\alpha = G/(nV_{\rm T})$).

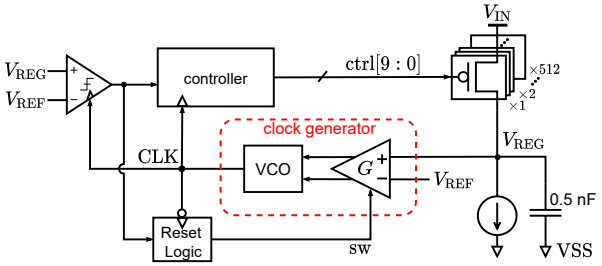

Fig. 2: Block diagram of the proposed LDO.

$G\Delta V_{\rm REG}$. The sum of the currents can then be expressed as a function of $\Delta V_{\rm REG}$ as follows.

$$I_{\rm p}+I_{\rm n} = I'_{\rm s}\left\{\exp\left(\frac{G\Delta V_{\rm REG}}{nV_{\rm T}}\right)+\exp\left(\frac{-G\Delta V_{\rm REG}}{nV_{\rm T}}\right)\right\} = 2I'_{\rm s}\left\{1+\frac{x^2}{2!}+\frac{x^4}{4!}+\ldots\right\}. \quad (2)$$

Here, $I'_{\rm s} = I_{\rm s}\exp\{(V_{\rm IN}/2 - V_{\rm th})/(nV_{\rm T})\}$ and $x = G\Delta V_{\rm REG}/(nV_{\rm T})$. Therefore, the clock frequency becomes a non-linear symmetric function of $\Delta V_{\rm REG}$.

As will be shown in Sec. III-A, the offset voltages of the output signals of the preamplifier, $V_{\rm a\_p,o}$ and $V_{\rm a\_n,o}$ change in the same direction under global variation. As a result, the VCO generates the minimum frequency when $\Delta V_{\rm REG}$ is close to 0. The preamplifier gain G suppresses the effects of random mismatch. Therefore, this built-in non-linear VCO generates a clock signal whose frequency is a non-linear symmetric function of $\Delta V_{\rm REG}$ and achieves robustness against PVT (process, voltage, and temperature) variations.

B. Overall Architecture

The overall architecture of our proposed LDO is shown in Fig. 2. It consists of a clock generator, a reset logic, a controller, a clocked comparator, and binary sized power MOSFETs. The clock generator generates the adaptive clock based on $\Delta V_{\rm REG}$. The comparator detects the polarity, based on which the controller controls the power MOSFETs. Reset logic generates a signal for the preamplifier to sample $V_{\rm REF}$.

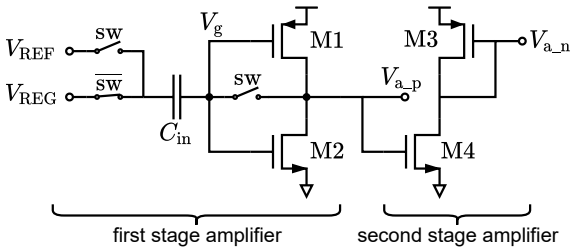

Fig. 3: Schematic of preamplifier.

C. Comparator

We use a StrongARM latch comparator as the clocked comparator [13]. The output voltage will be regulated to $V_{\rm REF}+V_{\rm offset}$ where $V_{\rm offset}$ is the comparator offset voltage. If this $V_{\rm offset}$ is large, it will have large voltage error $\Delta V_{\rm REG} = V_{\rm offset}$ in the steady-state. Furthermore, large $\Delta V_{\rm REG}$ causes high clock frequency in the steady-state. Thus, keeping the offset voltage as small as possible is essential.

D. Preamplifier

Differential input signals are required for the pMOSFET pair to generate a symmetric output current against output voltage error. We thus use a preamplifier with differential output. As the small signal input of the preamplifier is single ended, we adopt a two stage amplifier topology to generate the differential signals. The first stage has a gain of $-G$ and the second stage has a gain of -1. We adopt an inverter-based amplifier topology for the first stage [14]. This topology provides low-power and wide supply voltage operation. There are two modes of operation for this amplifier. One is the reset mode where the reset switch is turned ON. The other is the amplifying mode where the reset switch is turned OFF. Although the reset operation can be performed occasionally, the reset time should be small enough not to degrade the transient response. The second stage amplifier with gain -1 is realized by a common-source topology with diode load. The output offset voltages of both of the amplifiers become half of $V_{\rm IN}$ in typical condition.

When the "sw" signal is HIGH, the input voltage of the capacitor becomes $V_{\rm REF}$. The input and output of the inverter are shorted and they settle at the logical threshold voltage $V_{\rm a\_p,o}$ which is close to $V_{\rm IN}/2$. During this state, the voltage $V_{\rm Cin}$ across the input capacitor becomes $V_{\rm Cin} = V_{\rm a\_p,o} - V_{\rm REF}$. When the "sw" signal is LOW, the input voltage of the capacitor becomes $V_{\rm REG}$. The input and output of the inverter are opened so that the inverter's input voltage $V_{\rm g}$ becomes

$$V_{\rm g} = V_{\rm REG} + V_{\rm Cin} = V_{\rm REG} - V_{\rm REF} + V_{\rm a\_p,o}. \quad (3)$$

The voltage difference $V_{\rm REG} - V_{\rm REF}$ is then amplified with gain $-G$. As gate leakage current may change the voltage over time, periodic reset of the switches will be applied.

The gain of the second stage amplifier is $\Delta V_{\rm a\_n}/\Delta V_{\rm a\_p} = -g_{\rm mn}/g_{\rm mp}$. The gain is -1 when the transconductances $g_{\rm mn}$ and $g_{\rm mp}$ are the same. Thus $\Delta V_{\rm a\_p}$ and $\Delta V_{\rm a\_n}$ have opposite polarities to realize the symmetric frequency.

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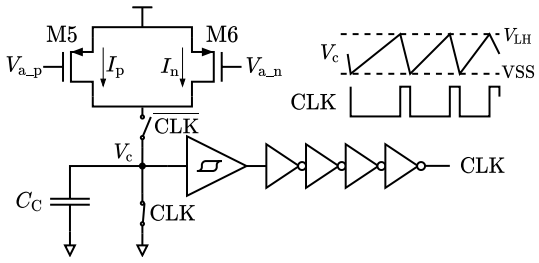


Fig. 4: Relaxation oscillator based non-linear VCO.

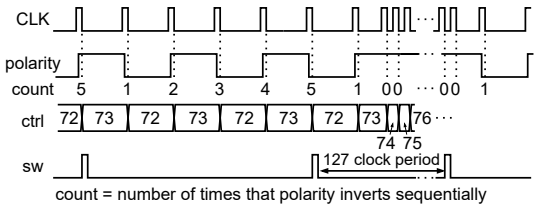


Fig. 5: Timing chart of control and reset logic.

E. VCO

Fig. 4 shows the schematic of the VCO. This VCO changes its frequency based on the sum of the currents provided by the pMOSFET pair. The frequency can be expressed as follows.

$$f_{\rm clk} = \frac{I_{\rm p} + I_{\rm n}}{C_{\rm c} \cdot V_{\rm LH}}. \tag{4}$$

Here, $C_{\rm C}$ is the load capacitance and $V_{\rm LH}$ is the upper threshold voltage of the Schmitt trigger. We can set the appropriate value of $C_{\rm C}$ for the target frequency range. Small $C_{\rm C}$ realizes fast transient response at the expense of higher quiescent current and vice versa.

F. Controller and reset logic

Digital LDOs suffers from LCO (limit cycle oscillation) because there is a 1 clock delay between polarity sampling and control signal generation [15]. To prevent LCO, we propose the following control scheme. At the positive clock edge, the controller samples the previous control value and the comparator output. These values are then fed into an adder which updates the control signal for the power MOSFETs at the next negative clock edge. This way, the power MOSFETs are controlled with a small delay even when the clock frequency is low.

The timing chart for the control and reset signals are shown in Fig. 5. The reset logic waits until the polarity signal inverts sequentially within a certain period to secure that $V_{\rm REG}$ is regulated to $V_{\rm REF}$. The interval of two reset operations can be determined based on the generated clock frequency. In this design, reset signal "sw" is generated if the polarity inverts sequentially five times. In addition, "sw" is forcibly generated if the polarity does not change for 127 clock periods to re-sample $V_{\rm REG} - V_{\rm REF}$ so that correct comparison is ensured. The reset time can be set using the delay of an inverter chain. The design of the reset time is critical as it affects the worst-case transient response. In our design, we set the reset time smaller than the minimum clock period.

III. Effect of PVT variation

One key design issue is to make sure that the output voltage error which generates the minimum frequency $\Delta V_{\rm REG\_fmin}$ is close to zero. For example, assume that $V_{\rm offset}$ of the comparator is zero and $\Delta V_{\rm REG\_fmin}$ is 10 mV. In this situation, high frequency is generated in the steady-state, and settling time becomes long when the output voltage crosses $V_{\rm REF}+10$ mV. Therefore, it is important to suppress $\Delta V_{\rm REG\_fmin}$ under PVT variations for adaptive frequency tuning.

A. Global process variation and temperature change

To keep $\Delta V_{\rm REG\_fmin}$ close to zero, the differential output of the preamplifier should be zero when $\Delta V_{\rm REG}$ is zero. For simplicity, we consider that only threshold voltage changes under process and temperature variation. We also assume that $\beta = \mu C_{\rm ox} W/L$ of all the MOSFETs are the same. The preamplifier is designed such that $V_{\rm a\_p,o}$ and $V_{\rm a\_n,o}$ become as follows.

$$V_{\rm a\_p,o} = \frac{V_{\rm IN}}{2} - \frac{V_{\rm th1} - V_{\rm th2}}{2},\ V_{\rm a\_n,o} = \frac{V_{\rm IN}}{2} - \frac{V_{\rm th3} - V_{\rm th4}}{2}. \tag{5}$$

Here, $V_{\rm th1}, V_{\rm th2}, V_{\rm th3}$, and $V_{\rm th4}$ are the threshold voltage of M1, M2, M3, and M4, respectively. From Eq. (5), changes in offset voltages by global process variations become the same since $\Delta V_{\rm th1} = \Delta V_{\rm th3},\ \Delta V_{\rm th2} = \Delta V_{\rm th4}$. Thus the preamplifier generates zero differential output at $\Delta V_{\rm REG} = 0$. Similarly, we obtain zero differential output at different supply voltages. As will be shown in Sec. III-B, even if we use different threshold devices for the two amplifiers, $\Delta V_{\rm REG\_fmin}$ will be suppressed by the preamplifier gain.

B. Random mismatch

Assume that the offset voltages, $V_{\rm a\_p,o}$ and $V_{\rm a\_n,o}$ change to $V_{\rm a\_p,o} + \Delta V_{\rm a\_p,o}$ and $V_{\rm a\_n,o} + \Delta V_{\rm a\_n,o}$, respectively because of random mismatch. Threshold voltages of the MOSFET pair in the VCO also suffer from variability. Assuming the changes as $\Delta V_{\rm thp}$ and $\Delta V_{\rm thn}$, Eq. (2) can be written as below.

$$I_{\rm p} + I_{\rm n} = I'_{\rm s} \left\{ \exp\left(\frac{G\Delta V_{\rm REG} - \Delta V_{\rm a\_p,o} - \Delta V_{\rm thp}}{nV_{\rm T}} \right) + \exp\left(\frac{-G\Delta V_{\rm REG} - \Delta V_{\rm a\_n,o} - \Delta V_{\rm thn}}{nV_{\rm T}} \right) \right\}. \tag{6}$$

$I_{\rm p}$ and $I_{\rm n}$ shift in y direction because of variability as shown in Fig. 6. The $I_{\rm p}$ and $I_{\rm n}$ lines in the log scale have slopes of $\pm G/(nV_{\rm T})$, thus $\Delta V_{\rm REG\_fmin}$ can be written as below.

$$\Delta V_{\rm REG\_fmin} = \frac{\Delta V_{\rm a\_p,o} + \Delta V_{\rm thp} - \Delta V_{\rm a\_n,o} - \Delta V_{\rm thn}}{2G}. \tag{7}$$

Assuming that all the MOSFETs suffer from the same variability, the standard deviation of $\Delta V_{\rm REG\_fmin}$ can be expressed as $\sigma_{\Delta V_{\rm REG\_fmin}} = \sqrt{6}\,\sigma_{V_{\rm th}}/(2G)$. Assuming the standard deviation of threshold voltage to be 30 mV for near minimum size transistors [16], $\sigma_{\Delta V_{\rm REG\_fmin}}$ becomes only 1.2 mV when the gain G is 30. Thus, the effect of random mismatch is reduced by the preamplifier gain. Therefore, the symmetric characteristic of VCO frequency is ensured even under the presence of random mismatch thanks to the preamplifier gain.

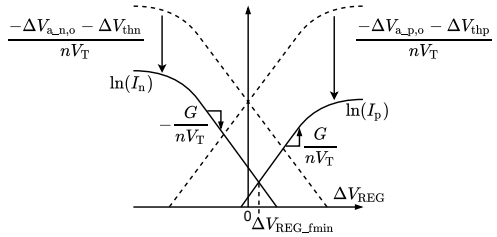


Fig. 6: Output voltage error and current.

TABLE I: Circuit design parameters.

$(W/L)_{M1}$	400 nm/200 nm, svt	$(W/L)_{M2}$	150 nm/200 nm, svt
$(W/L)_{M3}$	500 nm/500 nm, svt	$(W/L)_{M4}$	500 nm/120 nm, hvt
$(W/L)_{M5}$	300 nm/120 nm, hvt	$(W/L)_{M6}$	300 nm/120 nm, hvt
C_{in}	10 pF	C_c	1 pF

IV. Simulation Results

We design and layout our LDO in a commercial 65 nm low-power CMOS process. Fig. 7 shows the layout of the proposed LDO. We use HSPICE [17] to perform transistor-level simulations using foundry provided models. We evalute the quiescent current and transient response with post-layout simulation. The designed parameters of the MOSFETs are shown in Table I. We use a dropout voltage of 0.1 V for the demonstration.

A. Quiescent current

The quiescent current consists of a static component and a dynamic component. The dynamic component is proportional to clock frequency whereas the static component consists of the currents of the preamplifier and the VCO. At high-frequency region, dynamic power of the comparator and controller becomes dominant. At low-frequency region, the static component dominates and as such the quiescent current becomes a weak function of the frequency. The steady-state quiescent current is simulated to be 1.5 μA at $V_{IN} = 1.0$ V and 0.03 μA at $V_{IN} = 0.6$ V.

B. Process and temperature variation

Fig. 8(a) shows the output voltage error and generated clock frequency under different process corners of "TT", "FS", "SF", "SS", and "FF" at $V_{IN} = 1.0$ V. ΔV_{REG_fmin} does not change under different process corners. Fig. 8(b) shows the output voltage error and generated clock frequency under different temperature at $V_{IN} = 1.0$ V. ΔV_{REG_fmin} is close to 0 validating our proposed mechanism.

We then perform Monte Carlo simulation based on the foundry-provided statistical model. We simulate 300 virtual chips at $V_{IN} = 1.0$ V. The standard deviation of ΔV_{REG_fmin} is only 0.39 mV which confirms the suppression effect due to the preamplifier gain. Next, we evaluate the offset voltage variation of the latched comparator for 1023 virtual chips. The standard deviation of the offset voltage is 0.53 mV.

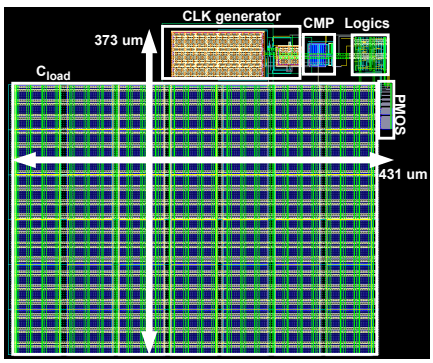
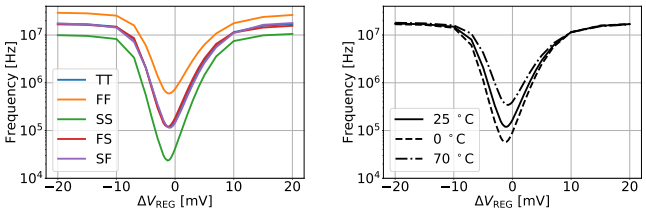


Fig. 7: Layout of the proposed LDO.



(a) Different process corners. **(b)** Different Temperature.

Fig. 8: Output voltage error and generated clock frequency.

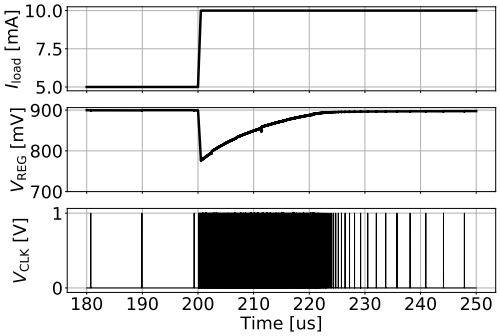


Fig. 9: Transient response with a 5–10 mA load change in 500 ns.

C. Transient response and current efficiency

This LDO operates across 0.6 to 1.2 V of input voltage. Fig. 9 shows the post-layout simulation result for a load current change of 5 mA to 10 mA with a time step of 500 ns and $V_{IN} = 1.0$ V. V_{REG} decreases when the load current increases and the clock frequency becomes higher accordingly. V_{REG} is thus regulated quickly and the clock frequency becomes lower again when the output voltage error becomes smaller. The clock frequency changes from 107 kHz to 14.5 MHz in this case and the voltage droop is 124 mV. Similar responses are obtained when the load current decreases. Fig. 10 shows the current efficiency for different input voltages and load currents. The current efficiency is above 96 % across a 50x load range. Average current efficiency under this range is 99.68 %.

D. Comparison with state-of-the-art techniques

Table II shows the comparison against other adaptive clocking techniques [9], [11], [18], [19]. We employ two figure of

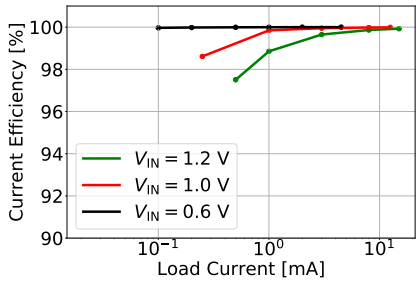


Fig. 10: Current efficiency at 0.1 V dropout.

TABLE II: Comparison table.

	This Work	[9]	[11]	[18]	[19]
Technology	65 nm	65 nm	65 nm	65 nm	65 nm
Built-in clock generation	Yes	No	Yes	Yes	Yes
Frequency range [MHz]	Continuous 0.1-14.5* (**135**×)	Discrete 50,500	Continuous 3.9- <70** (<17.9×)	Continuous NA	Cont.+Disc. 0.2-20 (100×), 70
V_{IN} [V]	0.6-1.2	0.6-1.1	0.6-1.2	0.65-1.2	0.5-1.0
V_{REG} [V]	0.5-1.1	0.4-1.0	0.4-1.1	0.6-1.15	0.45-0.95
I_{load} [mA]	~15	~100	~100	~30	~30
I_Q [uA]	**0.03-11 (1.5*)**	82	100-1070	9.8-180	10-169**
C_{load} [nF]	0.5	1	0.04	0.1	0.1
Max current efficiency [%]	**99.99***	99.92	99.5	99.4	99.93
V_{REG} droop	124 mV @5-10 mA, 500 ns	55 mV @2-100 mA, 20 ns	108 mV @20-70 mA, 800 ns	101.7 mV @10-30 mA, 0.1 ns	45 mV** @10-28 mA, 0.1ns
FOM1 [%]	**99.68**	NA	NA	NA	NA
FOM2 [ps]	3.72	0.47	1.38	4.58	2.35**

FOM1 = Average current efficiency across a 50× current dynamic range [8].
FOM2 = $(C_{load}\Delta V\ I_Q)/(\Delta I_{load})^2$. *: $V_{IN} = 1.0$ V, $V_{REG} = 0.9$ V. **: From figure.

merits (FOM) to compare both current efficiency and transient response capability. Proposed LDO realizes the smallest quiescent current and highest current efficiency. The average efficiency of more than 99 %. The speed FOM (FOM2) is 3.72 ps which is comparable to other reports. Thus, our LDO is suitable for low-power applications.

V. Conclusion

We proposed a digital LDO with built-in non-linear VCO for low quiescent current and fast transient response. The VCO operation consists of subthreshold current addition of a MOSFET pair and a preamplifier to ensure symmetric frequency characteristic under PVT variations without upsizing the MOSFETs. The quiescent current is 1.5 μA at 1.0 V of supply voltage, and the average current efficiency across a 50× range is 99.68 %. The proposed LDO can be adapted for both the low-power and high-performance applications by tuning the frequency range accordingly.

Acknowledgments

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